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Intel MB Schematic Document

2019 OMEN 17.3" Santorini

FPC72 LA-H492PR01

Date : 2018/09/28

Version: v0.1

15.6": FPC54 LA-H481PR(N17)
LA-H482P(N18)
17" : FPC72 LA-H491P(N17)
FPC72 LA-H492P(N18)

15" to 17" different:
01. Add SSD#2
02. Combo HP Jack to separated MIC jack
03. JDIMM2 to STD. revision.
04. Screw Location
05. BATT from SMT to DIP
06. ACIN CONN
07. GPU Core from 6phase to 4phase

(Modified&Ref from: 01."DPF50_LA-F842PR1A_201800411(PPAV)")
02.GPU:"DPF50_LA-F863PR01_180723(PPAV)")
03.GPU reference:"EH78F_LA-G161PR01_0810")

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Title	Cover Page		
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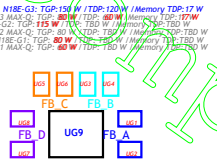
Model Name : OMEN N18E-G3

File Name :



UG108 OVR-M NCP45491XMNTWG P.22

UG2,UG1 8Gb_256Mx2Chx16 :2pcs P.35 — FBA x64

UG4,UG3 8Gb_256Mx2Chx16 :2pcs P.35 — FBB x64

UG6,UG5 8Gb_256Mx2Chx16 :2pcs P.36 — FBC x64

UG8,UG7 8Gb_256Mx2Chx16 :2pcs P.36 — FBD x64

UG9 GPU nVidia N18E-G3
256bits Two Channelsx16 (single sided)
37.5mm x 37.5mm P.27-34
*GB4B-256

PEG x16 P.9

UC1 Intel Coffee Lake- H 6C+GT2 P.7 P.8
TDP: 45W
42mm x 28mm
BGA 1440-Pin
14nm
0.65mm Ball Pitch
1 Die
6+2:16.5x9.1mm
8+2:19.4x9.1mm
P.6~13
P.9

DDR4_1.2V Interleaved (*1DPC)

AREA BACK
Ch0 (REV.) DDR4 SO-DIMM JDIMM1 P.23
Ch1 (STD.) DDR4 SO-DIMM JDIMM2 P.24
AREA FRONT
*(17" Ch1:JDIMM2 is REV. type)

JHDMI1 HDMI Conn. P.40 — HDMI Redriver PS8409 P.40 (UV3) — HDMI 2.0 — IFPC

JmDP1 Mini_DP Conn. P.39 — DP Repeter TUSB546 P.40 (UV43) — DP 1.4 — IFPA

JEDP1 eDP Conn. P.38 — eDP — IFPD

x4 DMI 3.0 P.16

UH1 HM370
Cannon Lake PCH-H
24mm x 25mm
BGA 874-Pin
0.5mm Ball Pitch
P.14 P.17 P.18 P.16 P.14~21

JRJ45 RJ-45 P.51 — GLAN RTL8118AS P.51 (UL1) — x1, Port #14 — PCIe

JUSB1 USB3.0 Conn.
UR1 Card Reader RTS5237S-GRT — x1, Port #15
HDD LED
JIO1 I/O Conn. P.71
US1 USB Charger TPS2546 P.71 — USB 2.0 Port #1
USB 3.0 Port #1
x1, Port #15

JWLAN1 WLAN+BT (M.2 Key E) P.52 — CNVi
USB 2.0 Port #14
x1, Port #16

JSSD1 SSD#1 (M.2 Key M) P.67 — x4, Port #12/11/10/9 (SATA#1A)

JSSD2 SSD#2 (M.2 Key M) P.68 — *for 17" only — x4, Port #21/22/23/24 (SATA#4)

PJP1 ACIN Conn. P.82
JPWR1 PWR BTN Conn.
JKBL1 KBL Conn. P.63
PUB01 Charger P.84
PJPB1 Battery Conn. P.83
U9 G-Sensor HP2DCTR P.66
JHDD1 2.5" HDD P.67 — SATA Port #0b

UK1 EC ENE KB9542Q-B P.58
SMBus#1
SMBus#2
LPC
ESB
PS2#3
SMBus

UG9 GPU P.25
JKB1 Int. KBD P.63
JFAN1 JFAN2 FAN P.77
U7 Hall Sensor P.63
UC3 Thermal Sensor P.66
JTP1 Touch Pad P.63
SPI

JLB1 RGB Conn. P62
UE1 RGB LED Driver TLC59116 P62
UK2 Extend I/O KC3810 P.59
UT1 TPM 2.0 SLB9670VQ2.0 P.66
UH2 BIOS 16MB W25Q128JVSIQ P.16

JTAG1 Debug
UT11 DP Repeter TUSB546 P.47 — GPU IFPE
U1 Thunderbolt Titan Ridge JHL7340 P.48 — PCIex4, Port #17/18/19/20
JUSBC1 USB Type-C P.50
UU4 Type-C PD TPS65987S P.50 — Port #4
UU5 SPI ROM W25X20CLSNIG P.50

USB 3.0
Port #2 — JUSB2 USB3.0 Conn. P.71
Port #3 — JUSB3 USB3.0 Conn. P.71
USB 2.0
Port #5 — JEDP1 HD/IR Camera P.38

HDA
UA1 Codec AL3292 P.56
JHP1 Combo Jack P.56
JMIC1 Stereo Mic Jack P.56 — *for 17" only
I2S
UAA1 ALC1305 P.57
JSPK1 Speaker Conn. P.57

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"OMEN17_BLOCK_DIAGRAM0817"

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
1 --> 0.2	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
2 --> 0.3	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
3 --> 0.4	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
4 --> 0.5					
5 --> 0.6					
6 --> 0.7					
7 --> 0.8					
8 --> 0.9					
9 --> 1.0					
10 --> 1.1					
11 --> 1.2					
12 --> 1.3					
13 --> 1.4					
14 --> 1.5					
15 --> 1.6					
16 --> 1.7					
17 --> 1.8					
18 --> 1.9					
19 --> 2.0					

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	---		
DDI2	---		
DDI3	---		
eDP	---		PCH_EDP_HPD_R

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM2	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x4F	0X9E	0X9F

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
SMBUS Port2	+3VL	PCH	TBC		
		GPU	0x4F	0X9E	0X9F
		THERMAL	0x48	0X90	0x91
		PD (Default)	0x38	0X70	0x71
		Type-C MUX	0x10 0x11	0X20 0X22	0x21 0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3V_PCH_PRIM				
I2C_1_SCL I2C_1_SDA	+3VS				

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
UMA	UMA@	
DIS	DIS@	
eSPI I/F	ESPI@	LPC@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@ VGAEMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1 Gen1/Gen2	1			USB3.1 Port 1		
1	USB3.1_2 Gen1/Gen2	2			USB3.1 Port 2		
2	USB3.1_3 Gen1/Gen2	3			USB3.1 Port 3		
3	USB3.1_4 Gen1/Gen2	4			USB Type-C Port		TBT
4	USB3.1_5 Gen1	5					
5	USB3.1_6 Gen1	6					
6	USB3.1_7 Gen1	7					
7	USB3.1_8 Gen1	8					
8	HM370 disable						
9	HM370 disable						
10	/ GbE						
11	HM370 disable						
12	HM370 disable						
13	HM370 disable						
14	PCIE_9 / GbE		9		SSD-1	CLK2 & CLKREQ#2	
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0			
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	Ethernet	CLK5 & CLKREQ#5	
20	PCIE_15		15		Card Reader	CLK3 & CLKREQ#3	
21	PCIE_16		16		WLAN	CLK1 & CLKREQ#1	
22	PCIE_17 / SATA_4		17	4	Thunderbolt	CLK0 & CLKREQ#0	
23	PCIE_18 / SATA_5		18	5			
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21		SSD-2 or Optane	CLK6 & CLKREQ#6	
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 Port 1
2	USB3.1 Port 2
3	USB3.1 Port 3
4	USB3.1 Type-C Port
5	
6	Camera/IR Camera
7	
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

GPU IFPx Table

Port	Function
A	mDP
B	--
C	HDMI 2.0
D	eDP
E	DP source to TBT
F	--

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

BOM Number	Load BOM Option
431AAN32L01	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNCT@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@
431AAN32L02	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNVH@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@

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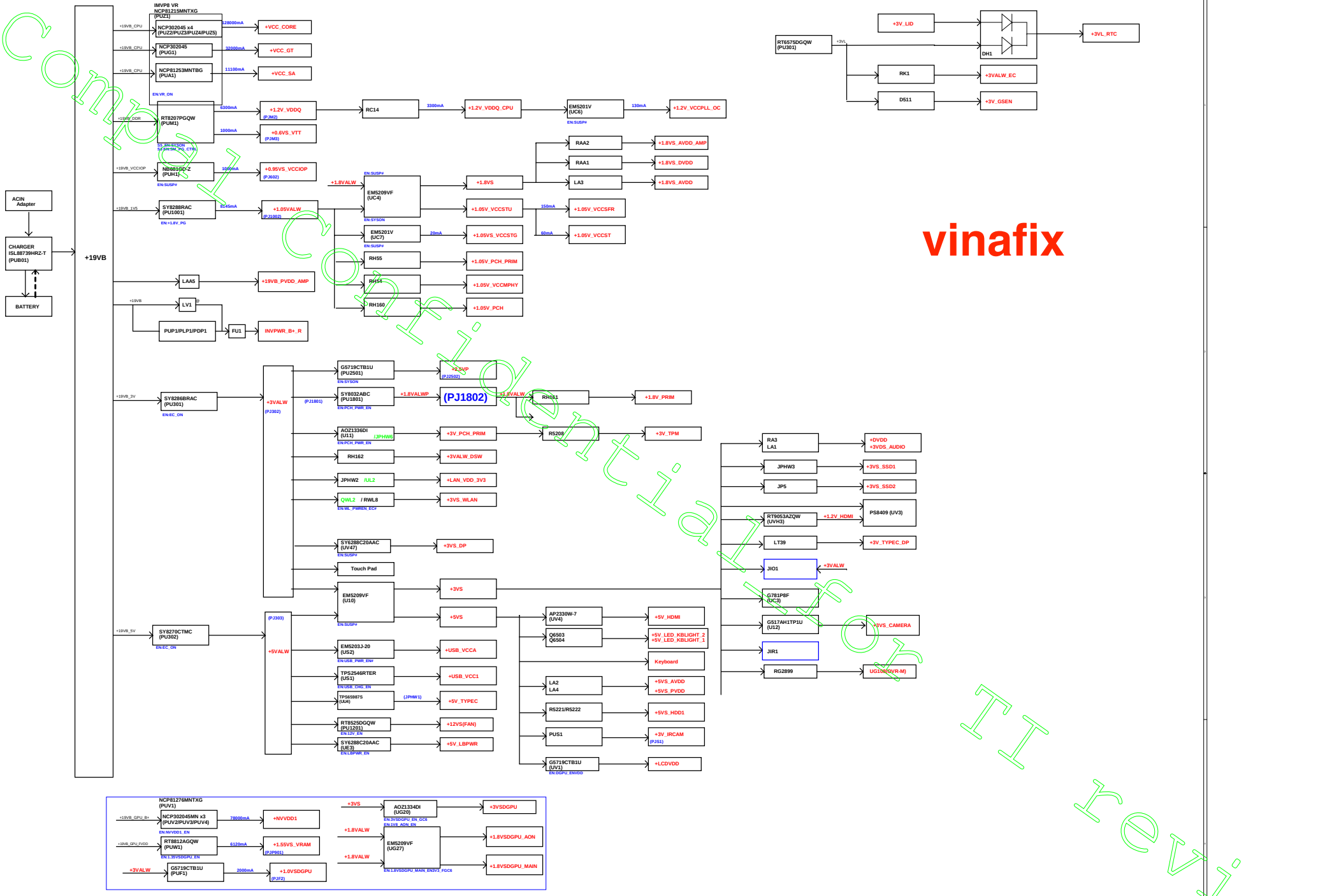

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			Power Map
		Document Number	Rev
		PPC54 LA-H482P	1A
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[DDX03 PWR Sequence_CFL-H 6+2_DDR4]

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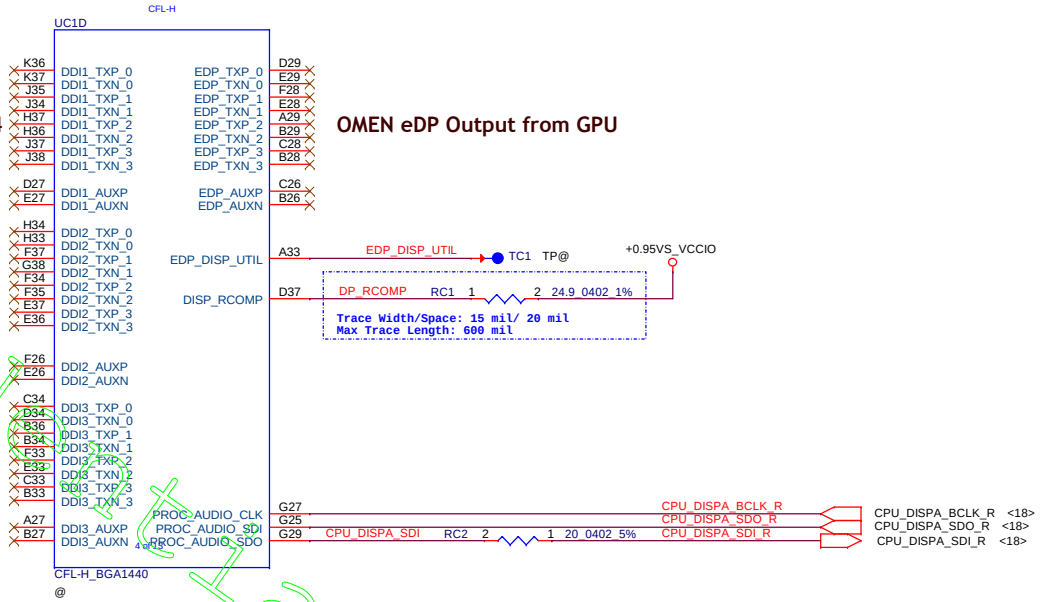
OMEN: TR DDI input from GPU for DP v1.4

OMEN eDP Output from GPU



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Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
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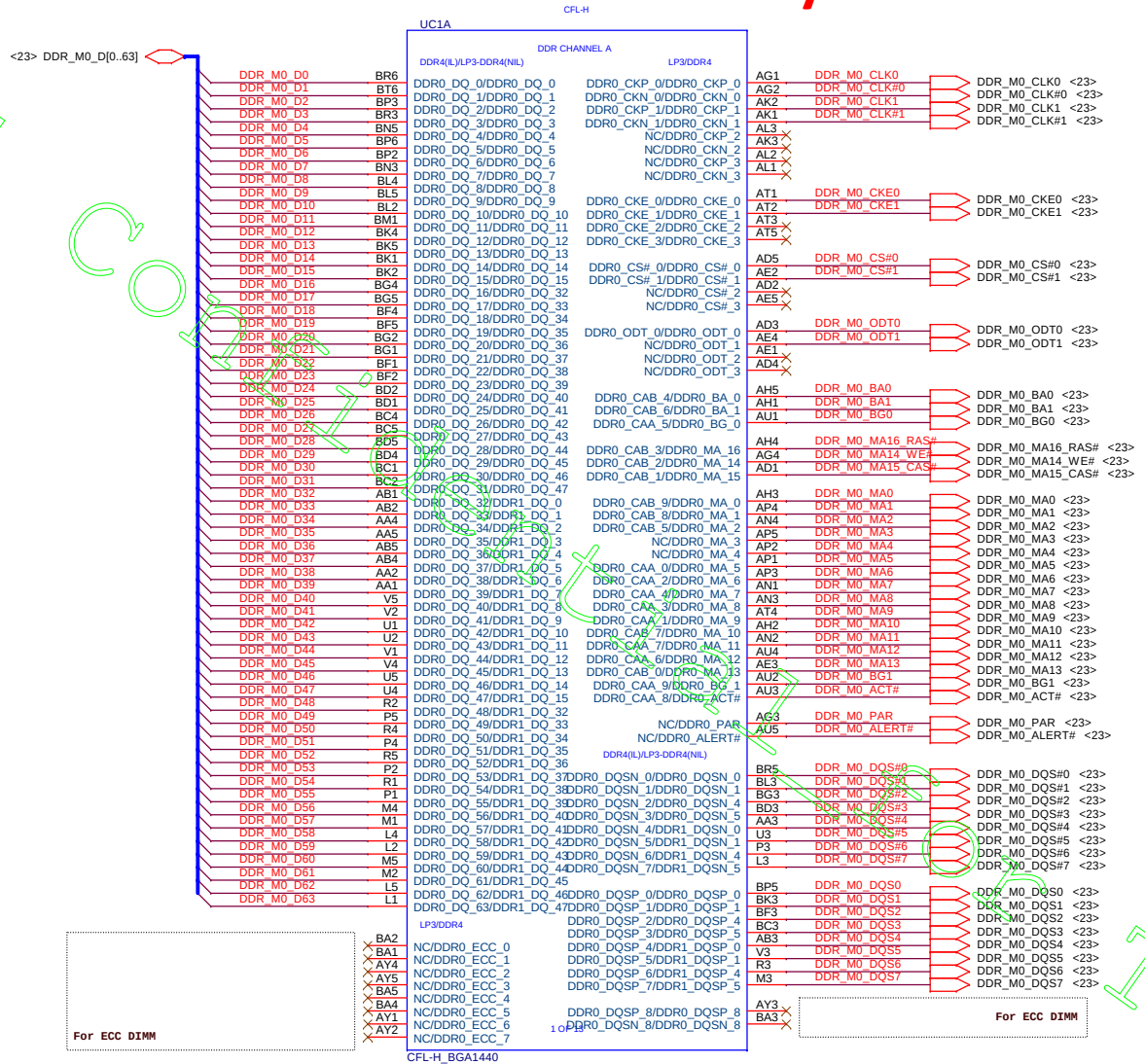
CHANNEL - A

Interleaved Memory



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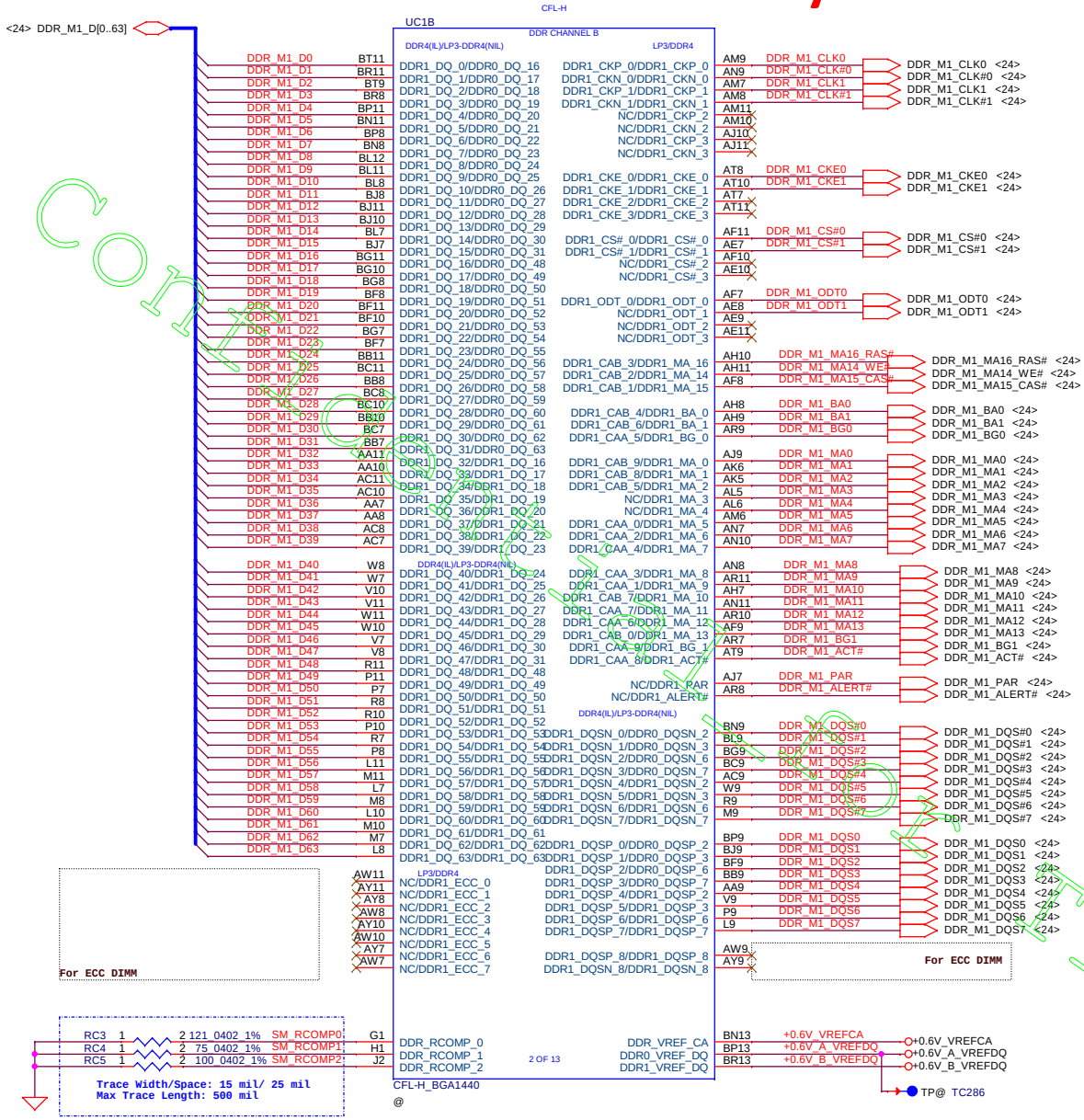
CHANNEL - B

Interleaved Memory



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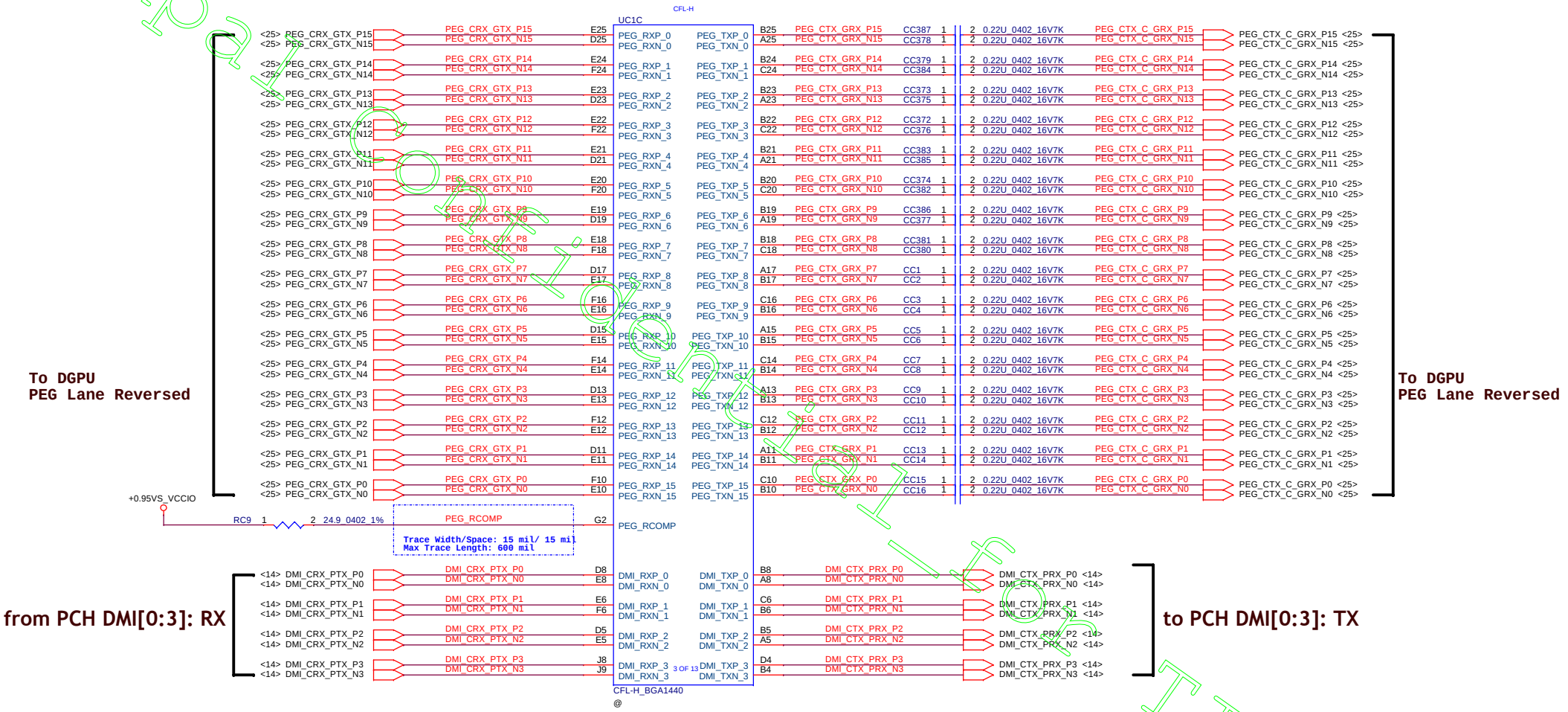

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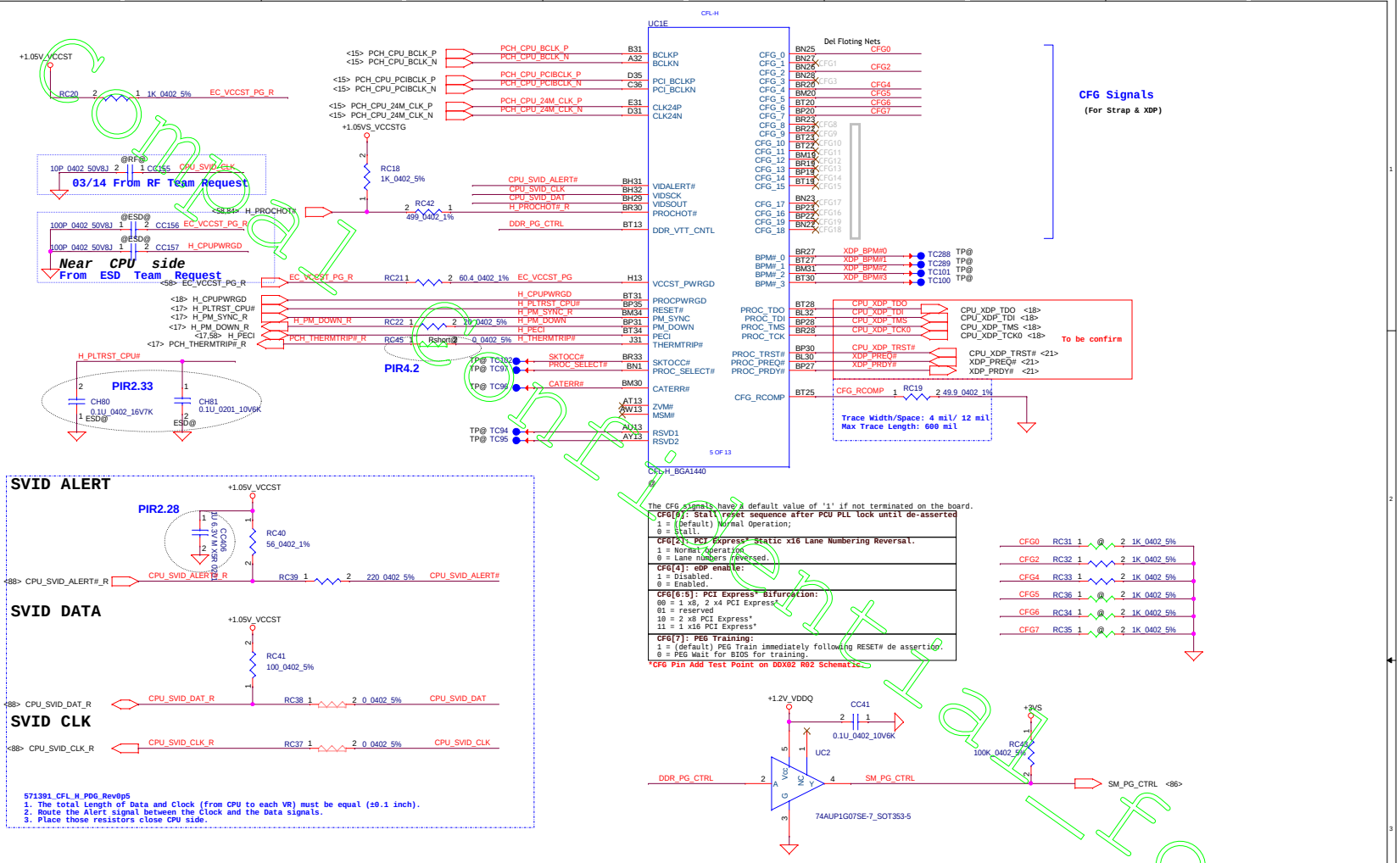

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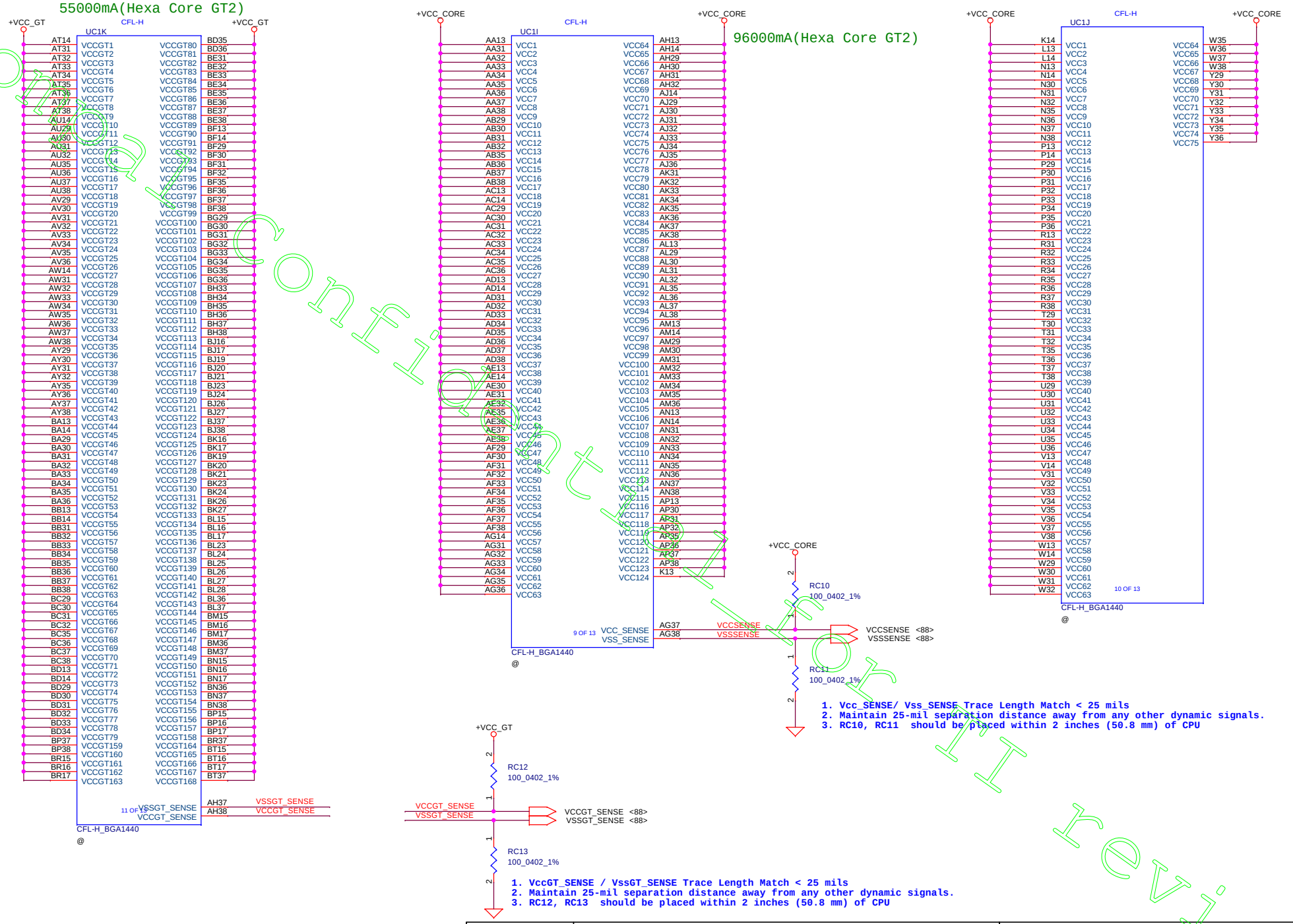

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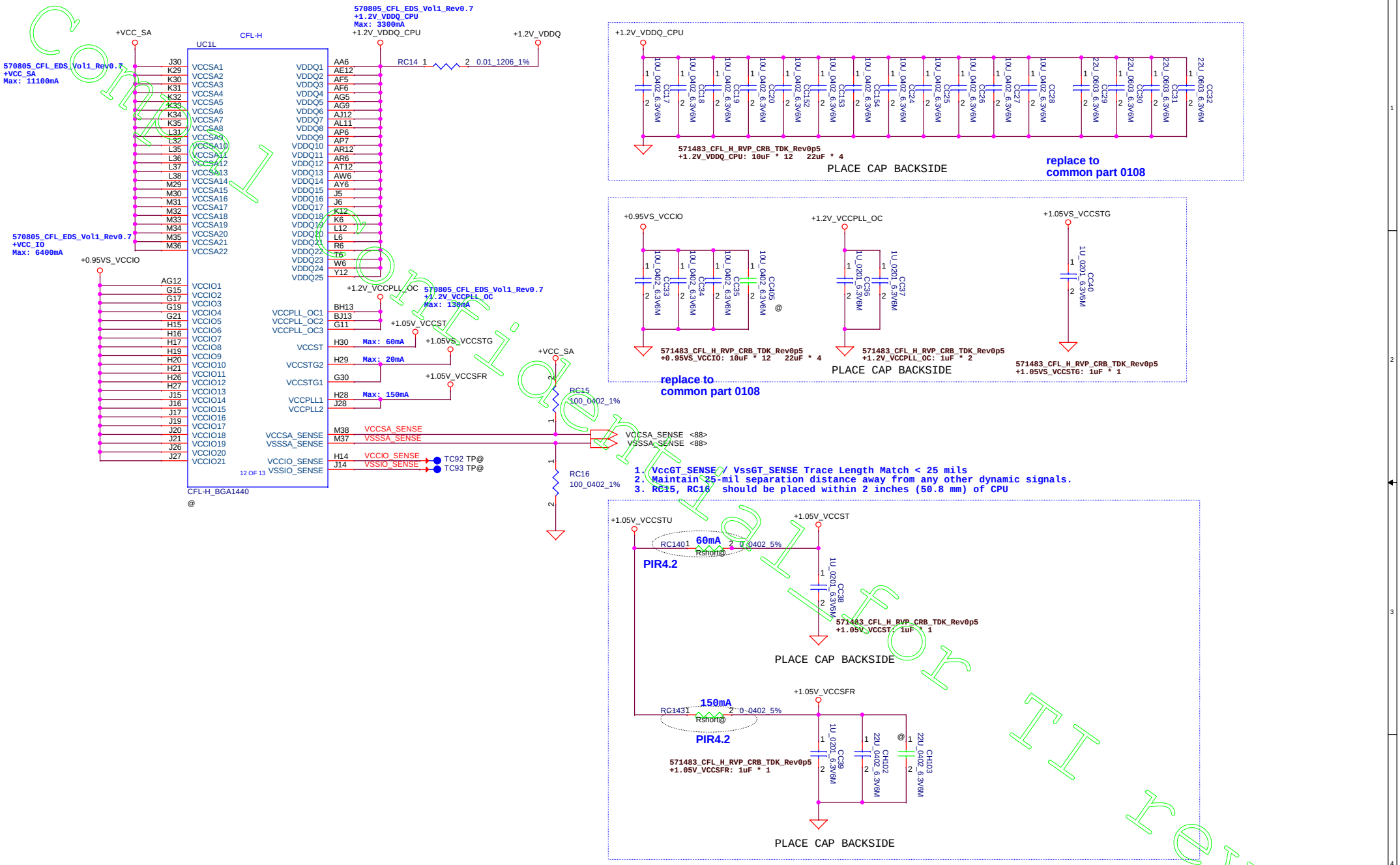

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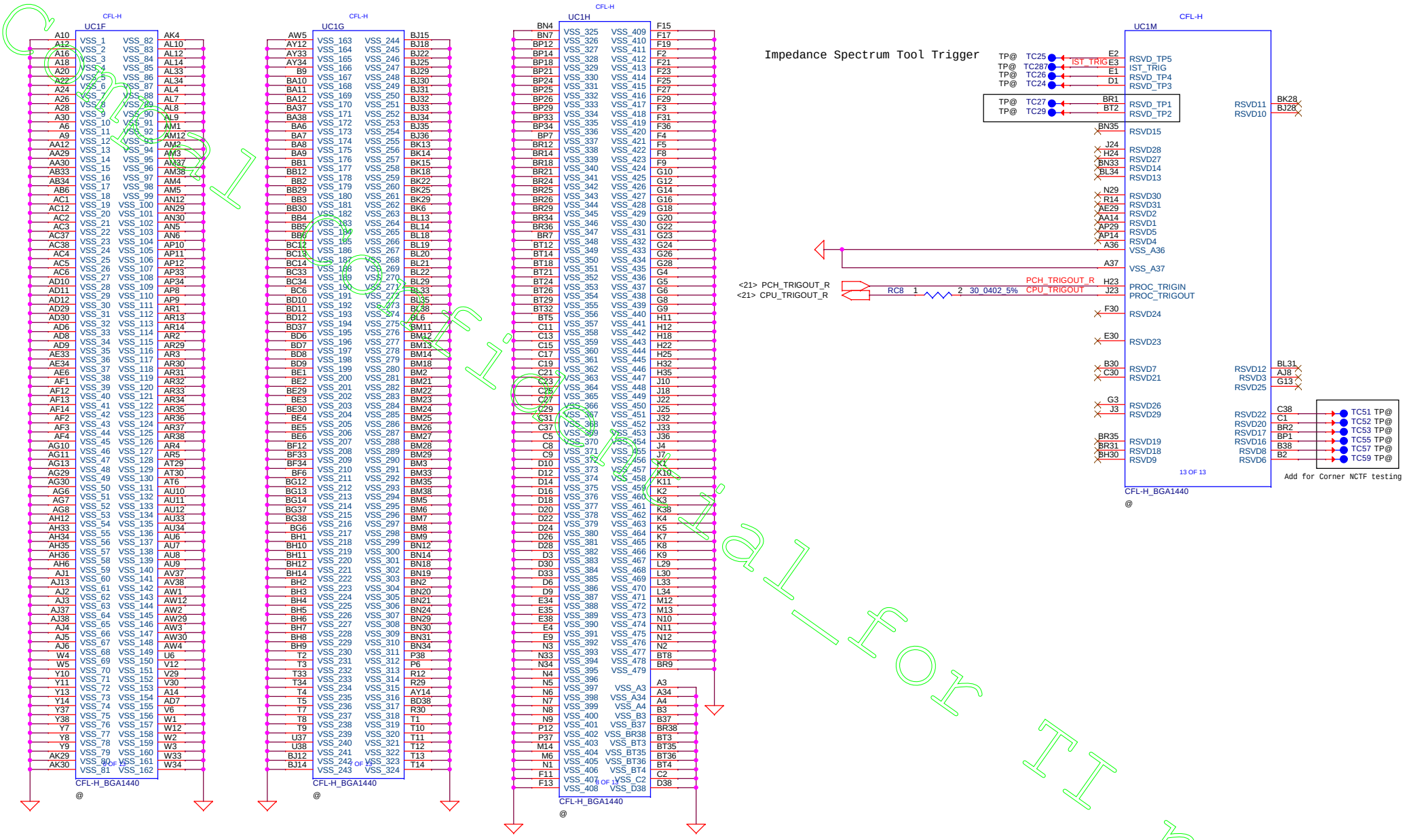

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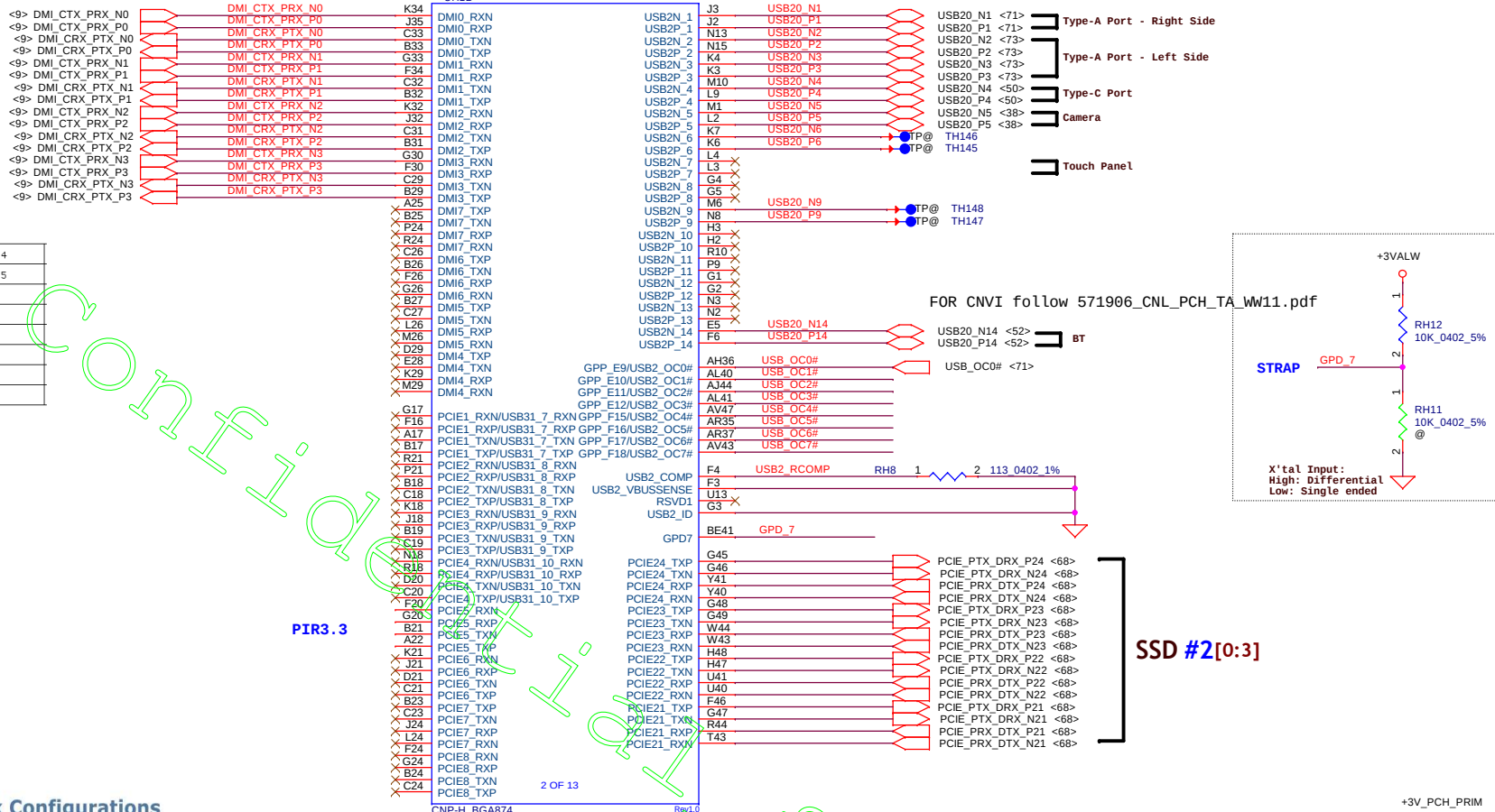
from/to CPU DMI[0:3]:RX/TX



Flex I/O Lane	HM370
0	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2
4	USB3.1 Gen1
5	USB3.1 Gen1
6	USB3.1 Gen1
7	USB3.1 Gen1
8	N/A
9	N/A
10	GbE
11	N/A
12	N/A
13	N/A
14	PCIe*, GbE
15	PCIe*
16	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B
20	PCIe*
21	PCIe*

PCIE Port 5

22	PCIe*, SATA 4
23	PCIe*, SATA 5
24	PCIe*
25	PCIe*
26	PCIe*
27	PCIe*
28	PCIe*
29	PCIe*

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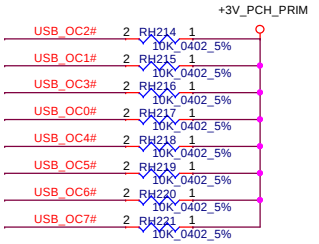
Figure 26-1. Supported PCI Express* Link Configurations

PCH-H Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 / Cycle Router #1				PCIe* Controller #4				PCIe* Controller #5 / Cycle Router #3				PCIe* Controller #6 / Cycle Router #2			
Flex I/O Lane #		6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HM370 HM375	1x4									RP 9 SSD#1				RP 13				SSD#2 RP 17				TR RP 21			
	1x4 LR									RP 9				RP 13				RP 17				RP 21			
	2x2									RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1									RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2									RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1									RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
QM370 QM375	1x4					RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR					RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2					RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1					RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2					RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1					RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
CM246 CM248	1x4	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
—A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
— PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
— A maximum of 6 SATA Ports (or devices) can be enabled
— SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
— SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
— A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
— A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
— x2 and x4 PCIe* NVMe SSD
— x2 IntelR Optane? Memory Device
— See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



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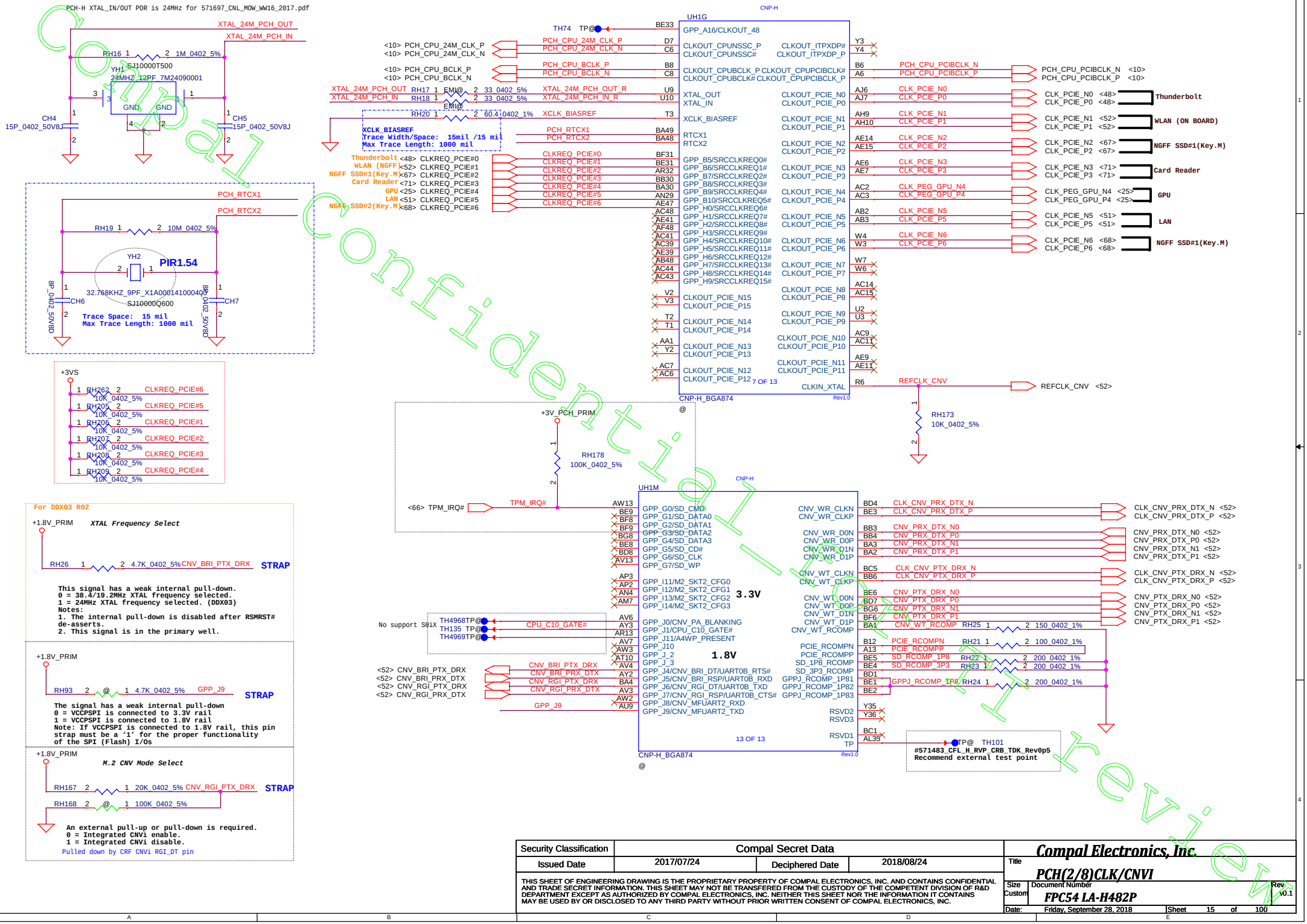

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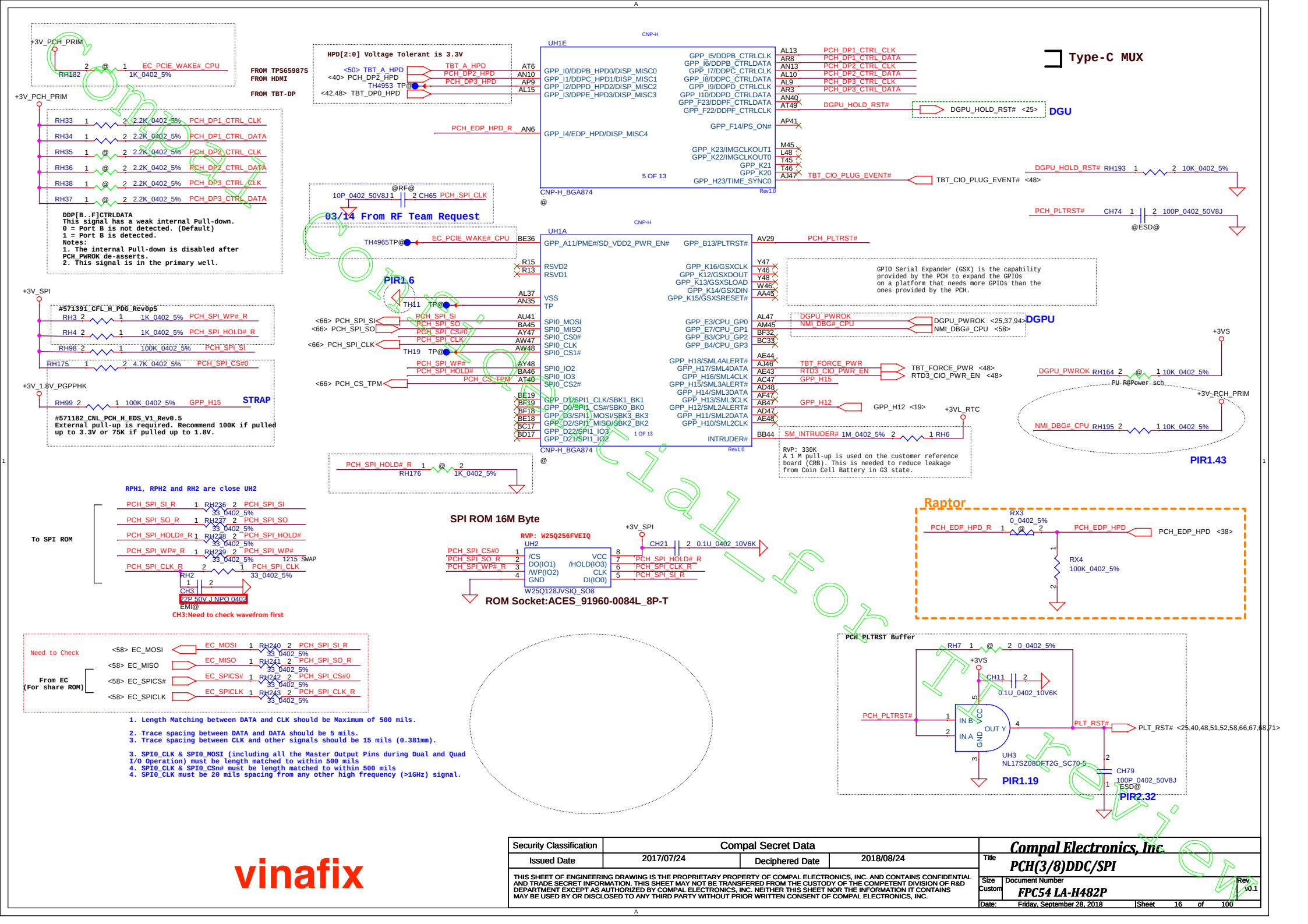

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Type-A Port :Left Side

Type-A Port :Right Side

I/O Board

USB#1

USB#2

SSD #1[2]

SSD #1[0:1]

SSD#1[3]

LAN

HDD

TBT:to Titan Ridge

Card Reader

WLAN

Titan Ridge

PIR4.2

PIR2.2

RH27&CH70 Need use after checking

RH166 close to PCH

3.2.1 Cannon Lake PCH-H

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Figure 3-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

RST	Flex I/O Lane	USB#/PCIe#/Gbe/SATA	
	0	#1/x/x/x	
	1	#2/x/x/x	
	2	#3/x/x/x	
	3	#4/x/x/x	
	4	#5/x/x/x	
	5	#6/x/x/x	
x	6	#7/ #1/x/x	
	7	#8/ #2/x/x	
x	8	#9/ #3/x/x	
	9	#10/ #4/x/x	
	10	x/#5/Gbe/x	
x	11	x/#6/x/x	
	12	x/#7/x/x	
	13	x/#8/x/x	
Yes	14	x/#9/Gbe/x	
	15	x/#10/x/x	SSD#1
	16	x/#11/x/#0a	
	17	x/#12/Gbe/#1a	
x	18	x/#13/Gbe/#0b	HDD
	19	x/#14/x/#1b	LAN
	20	x/#15/x/#2	CR
	21	x/#16/x/#3	WLAN
Yes	22	x/#17/x/#4	
	23	x/#18/x/#5	SSD#2
	24	x/#19/x/#6	
Yes	26	x/#21/x/x	
	27	x/#22/x/x	Titan Ridge
	28	x/#23/x/x	
	29	x/#24/x/x	

High Speed I/O (HSIO) Type and Lane	Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
		USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
								PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE			SATA 1a	SATA 0b	GbE	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7			
Intel® RST Support								No Support				No Support				Yes			No Support				Yes			Yes					
																RP#9							RP#17			RP#21					

HSIO Lane Assignments – Cannon Lake PCH-H

SKU

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA P0/P1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

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Figure 26-1. Supported PCI Express* Link Configurations

PCH-H Details	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3 (Cycle Router #1)	PCIe* Controller #4 (Cycle Router #1)	PCIe* Controller #5 (Cycle Router #3)	PCIe* Controller #6 (Cycle Router #3)
Flex I/O Lane #	6 7 8 9	10 11 12 13	14 15 16 17	18 19 20 21	22 23 24 25	26 27 28 29
PCIe* Lane #	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
HM370 / HM375	1x4		RP 9 (SSD#1)	RP 13	RP 17 (SSD#1)	RP 21 (TR)
	1x4 LR		RP 9	RP 13	RP 17	RP 21
	2x2		RP 9	RP 11	RP 13	RP 15	RP 17	RP 19	RP 21	RP 23
	1x2+2x1		RP 9	RP 11 RP 12	RP 13	RP 15 RP 16	RP 17	RP 19	RP 20	RP 21	RP 23	RP 24
	2x1+1x2		RP 12 RP 11	RP 9	RP 16 RP 15	RP 13	RP 20	RP 19	RP 17	RP 24	RP 23	RP 21
	4x1		RP 3	RP 10 RP 11 RP 12	RP 13	RP 14 RP 15 RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22 RP 23 RP 24
QM370 / QM375	1x4	RP 5		RP 9	RP 13		RP 17		RP 21	
	1x4 LR	RP 5		RP 9	RP 13		RP 17		RP 21	
	2x2	RP 5	RP 7	RP 9	RP 11	RP 13	RP 15	RP 17	RP 19	RP 21	RP 23	
	1x2+2x1	RP 5	RP 7 RP 8	RP 9	RP 11 RP 12	RP 13	RP 15 RP 16	RP 17	RP 19	RP 20	RP 21	RP 23 RP 24
	2x1+1x2	RP 8 RP 7	RP 5	RP 12 RP 11	RP 9	RP 16 RP 15	RP 13	RP 20	RP 19	RP 17	RP 24	RP 23	RP 21
	4x1	RP 5	RP 6 RP 7 RP 8	RP 3	RP 10 RP 11 RP 12	RP 13	RP 14 RP 15 RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22 RP 23 RP 24
CM246 / CM248	1x4	RP 1	RP 5	RP 3		RP 13		RP 17		RP 21	
	1x4 LR	RP 1	RP 5	RP 9		RP 13		RP 17		RP 21	
	2x2	RP 1	RP 3	RP 5	RP 7	RP 9	RP 11	RP 13	RP 15	RP 17	RP 19	RP 21	RP 23
	1x2+2x1	RP 1	RP 3 RP 4	RP 5	RP 7 RP 8	RP 9	RP 11 RP 12	RP 13	RP 15 RP 16	RP 17	RP 19	RP 21	RP 23 RP 24
	2x1+1x2	RP 4 RP 3	RP 1	RP 8 RP 7	RP 5	RP 12 RP 11	RP 9	RP 16 RP 15	RP 13	RP 20	RP 19	RP 17	RP 24	RP 23	RP 21
	4x1	RP 1	RP 2 RP 3 RP 4	RP 5	RP 6 RP 7 RP 8	RP 9	RP 10 RP 11 RP 12	RP 13	RP 14 RP 15 RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22 RP 23 RP 24

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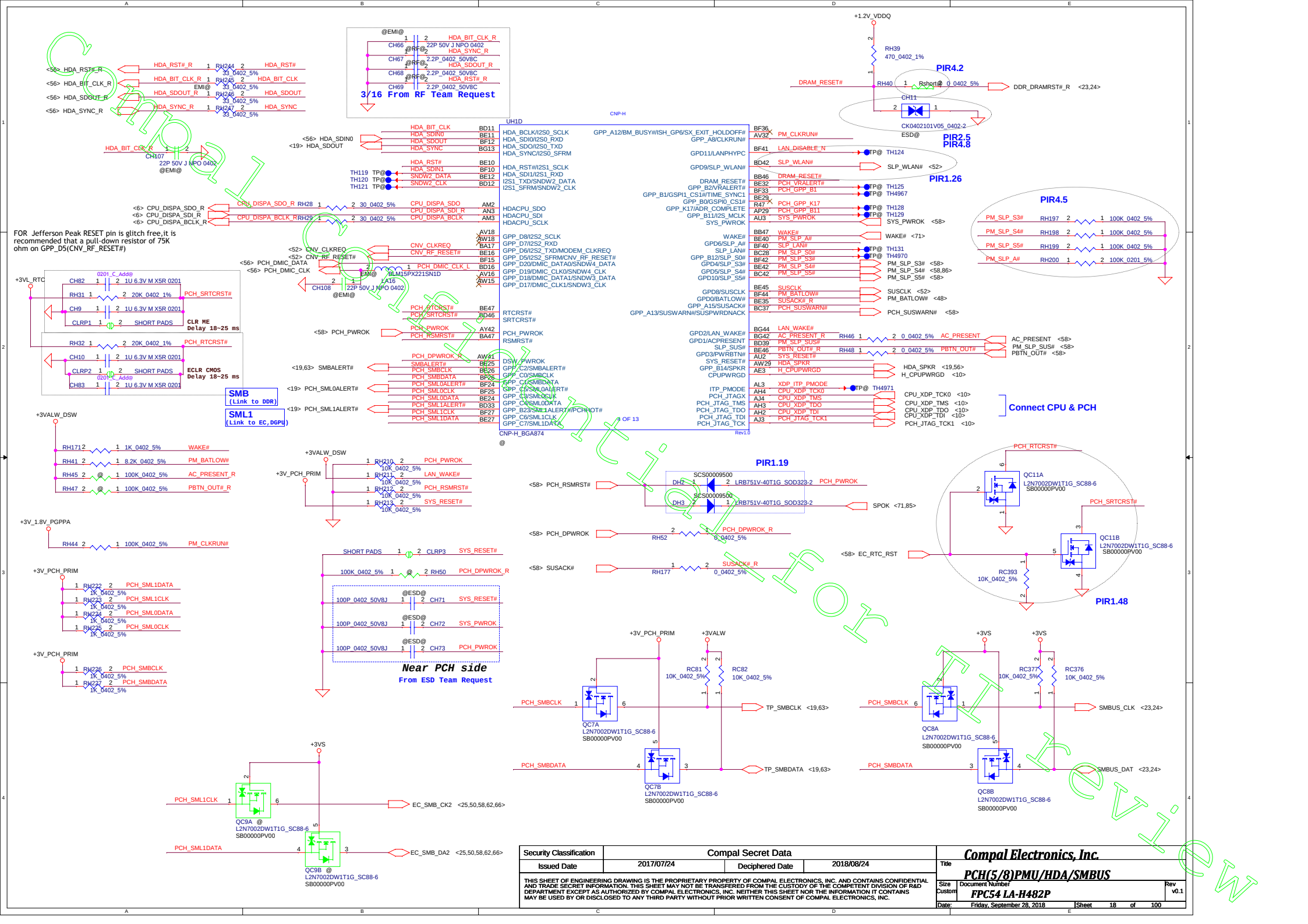
3/16 From RF Team Request
PIR4.2
PIR2.5
PIR4.8
PIR1.26
PIR4.5
PIR1.19
PIR1.48
Connect CPU & PCH
SMB
(Link to DDR)
SML1
(Link to EC,DGPU)
CLR ME
Delay 18~25 ms
ECLR CMOS
Delay 18~25 ms
FOR Jefferson Peak RESET pin is glitch free,it is recommended that a pull-down resistor of 75K ohm on GPP_D5(CNV_RF_RESET#)
Near PCH side
From ESD Team Request
CNP-H
UH1D
9 OF 13
CNP-H_BGA874
Rev1.0
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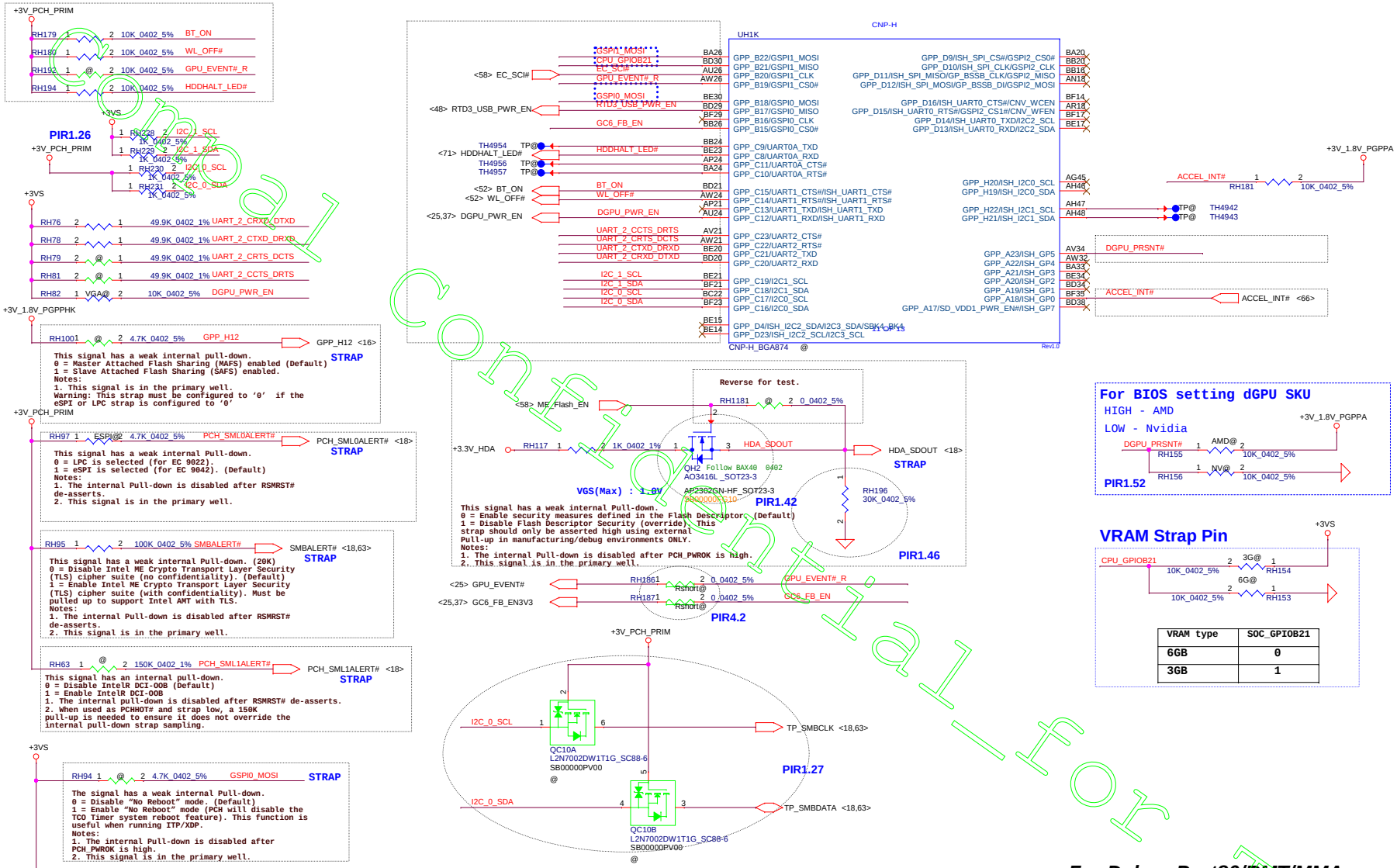

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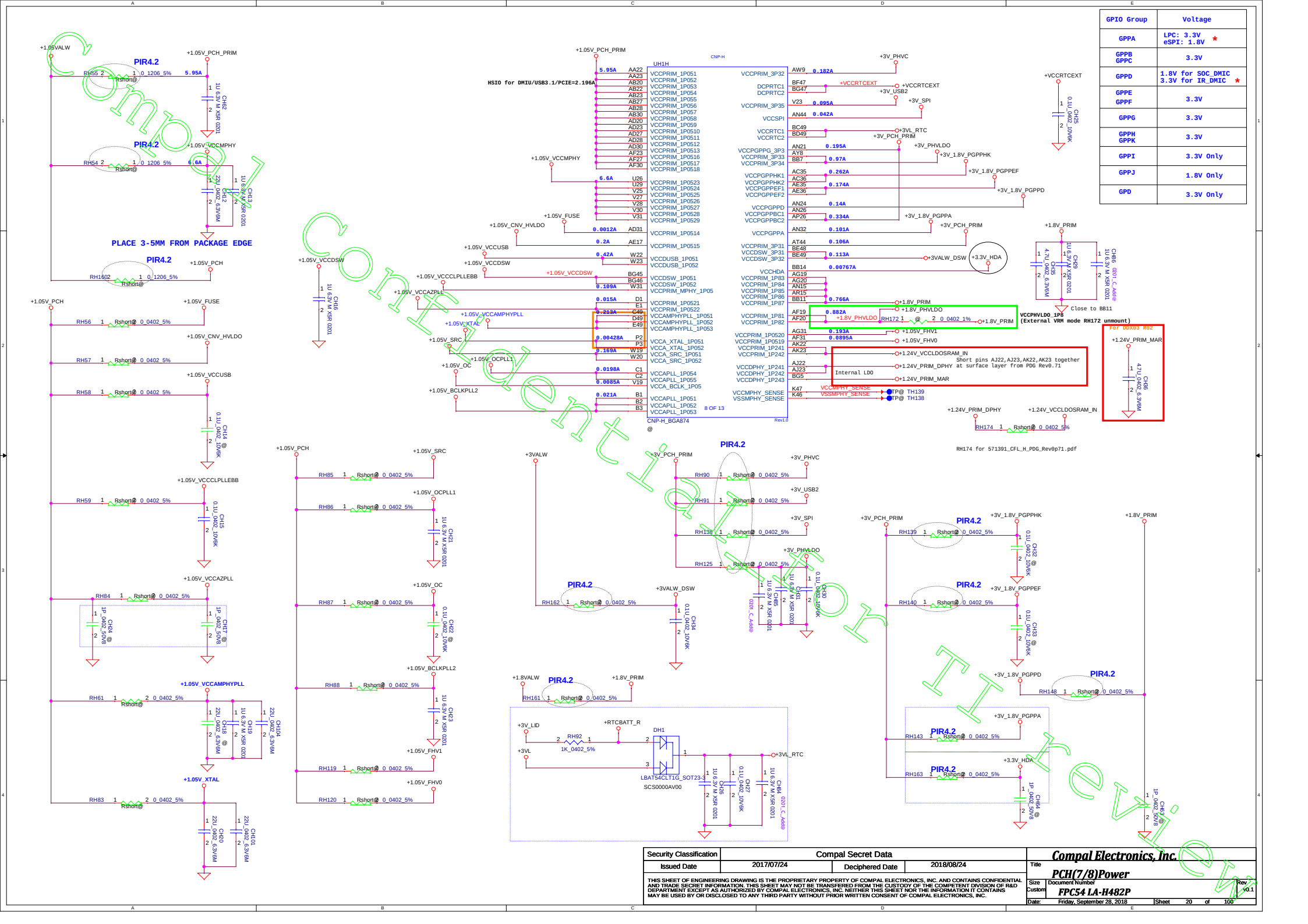

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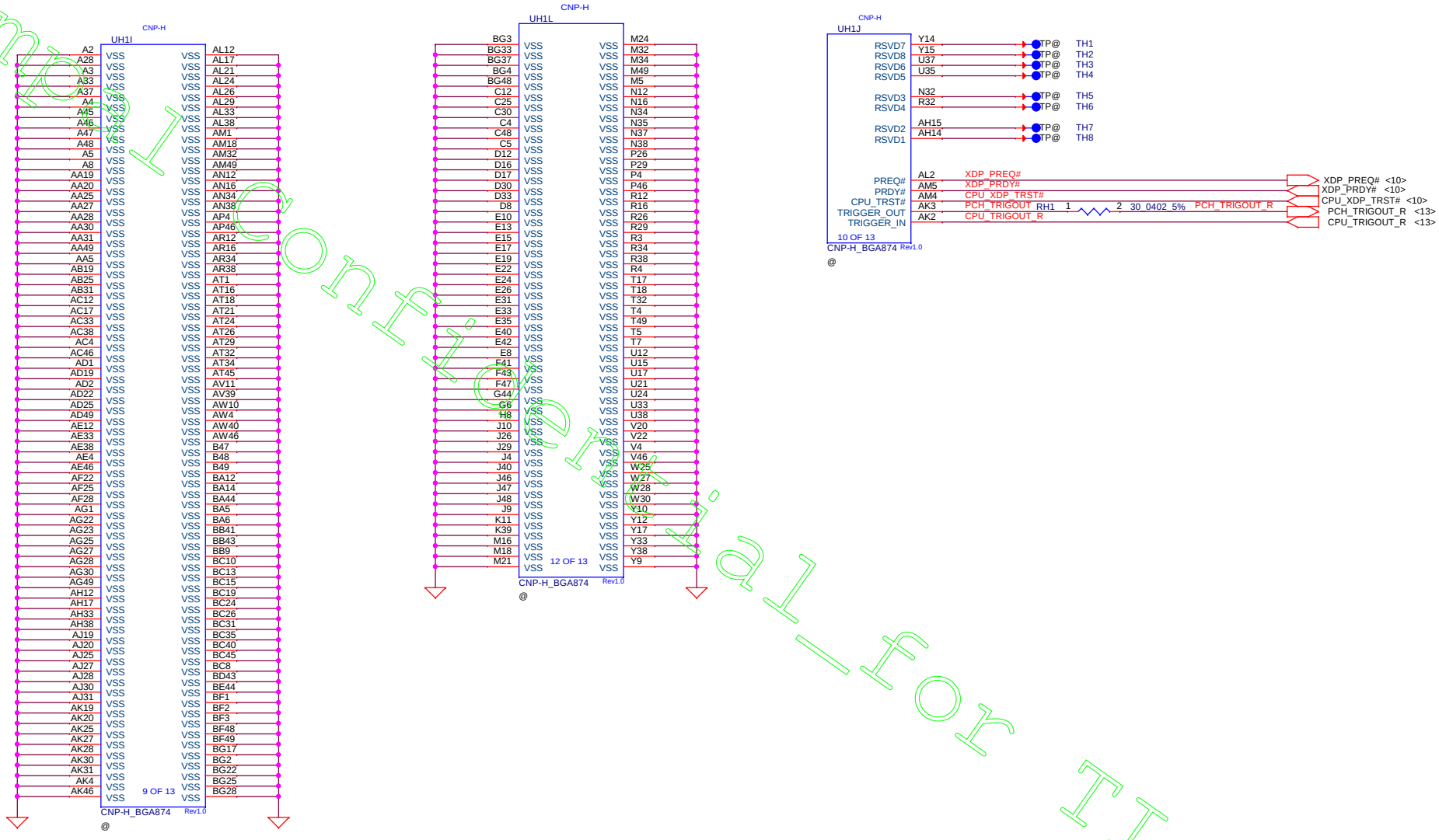
Custom	FPC54 LA-H482P		v0.1
Date:	Friday, September 28, 2018	Sheet	20 of 100



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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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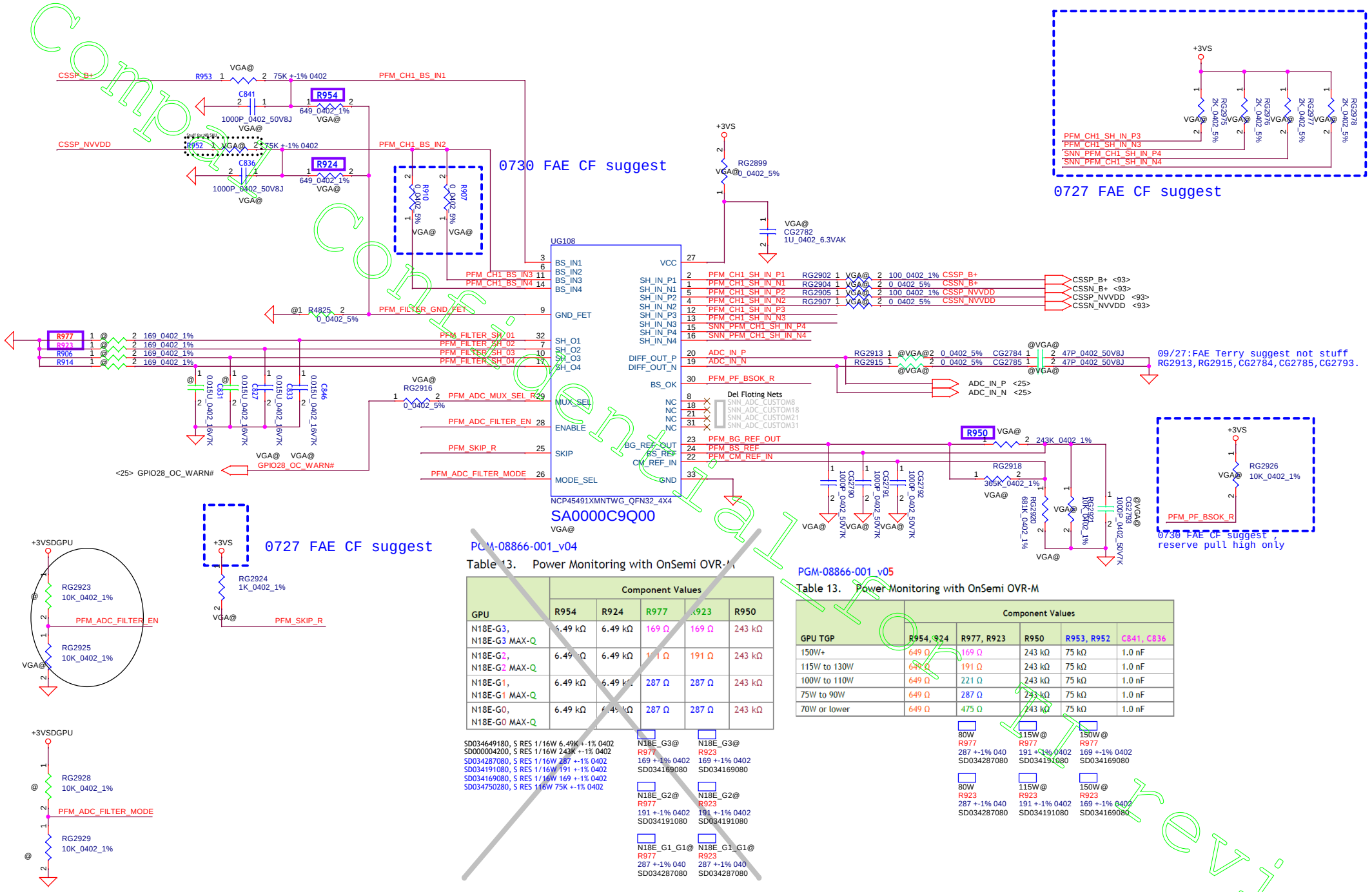
Compal Electronics, Inc.			
Title: PCH(8/8)GND/RSVD			
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 21 of 100		



GPU	Component Values				
	R954	R924	R977	R923	R950
N18E-G3, N18E-G3 MAX-Q	6.49 kΩ	6.49 kΩ	169 Ω	169 Ω	243 kΩ
N18E-G2, N18E-G2 MAX-Q	6.49 kΩ	6.49 kΩ	191 Ω	191 Ω	243 kΩ
N18E-G1, N18E-G1 MAX-Q	6.49 kΩ	6.49 kΩ	287 Ω	287 Ω	243 kΩ
N18E-G0, N18E-G0 MAX-Q	6.49 kΩ	6.49 kΩ	287 Ω	287 Ω	243 kΩ

SD034649180, S RES 1/16W 6.49K +-1% 0402
SD0000004200, S RES 1/16W 243K +-1% 0402
SD034287080, S RES 1/16W 287 +-1% 0402
SD034191080, S RES 1/16W 191 +-1% 0402
SD034169080, S RES 1/16W 169 +-1% 0402
SD034750280, S RES 1/16W 75K +-1% 0402

N18E_G3@ R977 169 +-1% 0402 SD034169080
N18E_G3@ R923 169 +-1% 0402 SD034169080
N18E_G2@ R977 191 +-1% 0402 SD034191080
N18E_G2@ R923 191 +-1% 0402 SD034191080
N18E_G1_G1@ R977 287 +-1% 040 SD034287080
N18E_G1_G1@ R923 287 +-1% 040 SD034287080

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

80W R977 287 +-1% 040 SD034287080
115W@ R977 191 +-1% 0402 SD034191080
150W@ R977 169 +-1% 0402 SD034169080
80W R923 287 +-1% 040 SD034287080
115W@ R923 191 +-1% 0402 SD034191080
150W@ R923 169 +-1% 0402 SD034169080

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Issued Date	2017/11/23	Deciphered Date	2018/09/01

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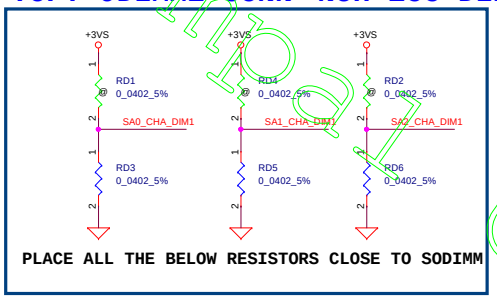
Compal Electronics, Inc.			
Title: OVR-M			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Friday, September 28, 2018	Sheet 22 of 100		

CHANNEL-A

REVERSE TYPE (4 mm)

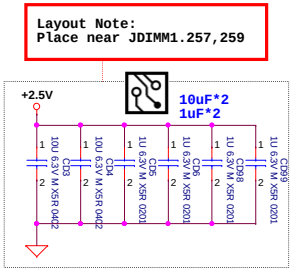
Interleaved Memory

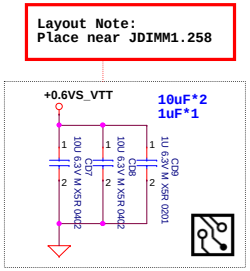
TOP: JDIMM1 CONN Non-ECC DIMM

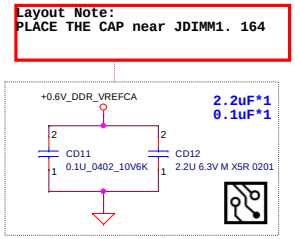


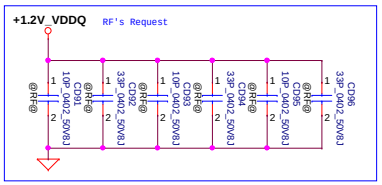
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

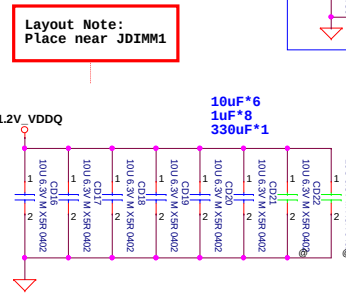
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

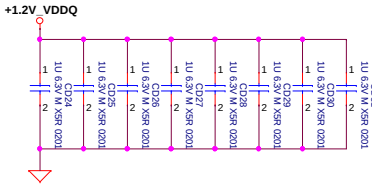


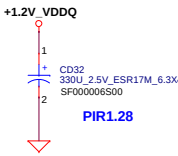


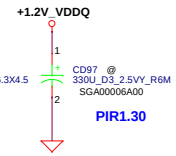


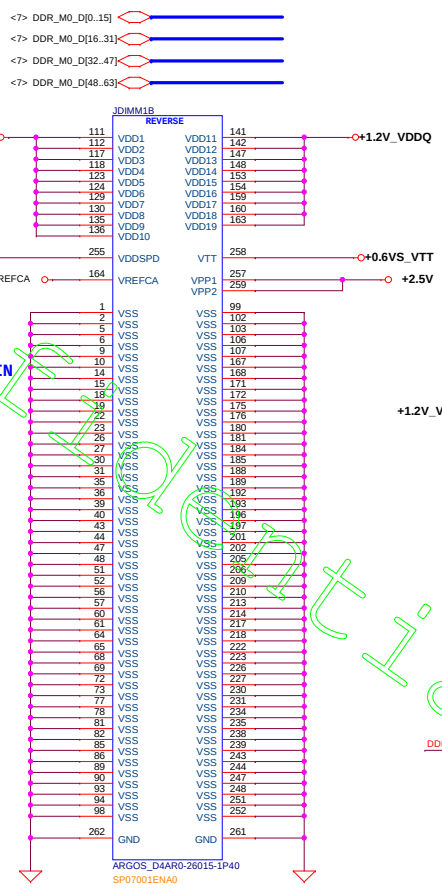


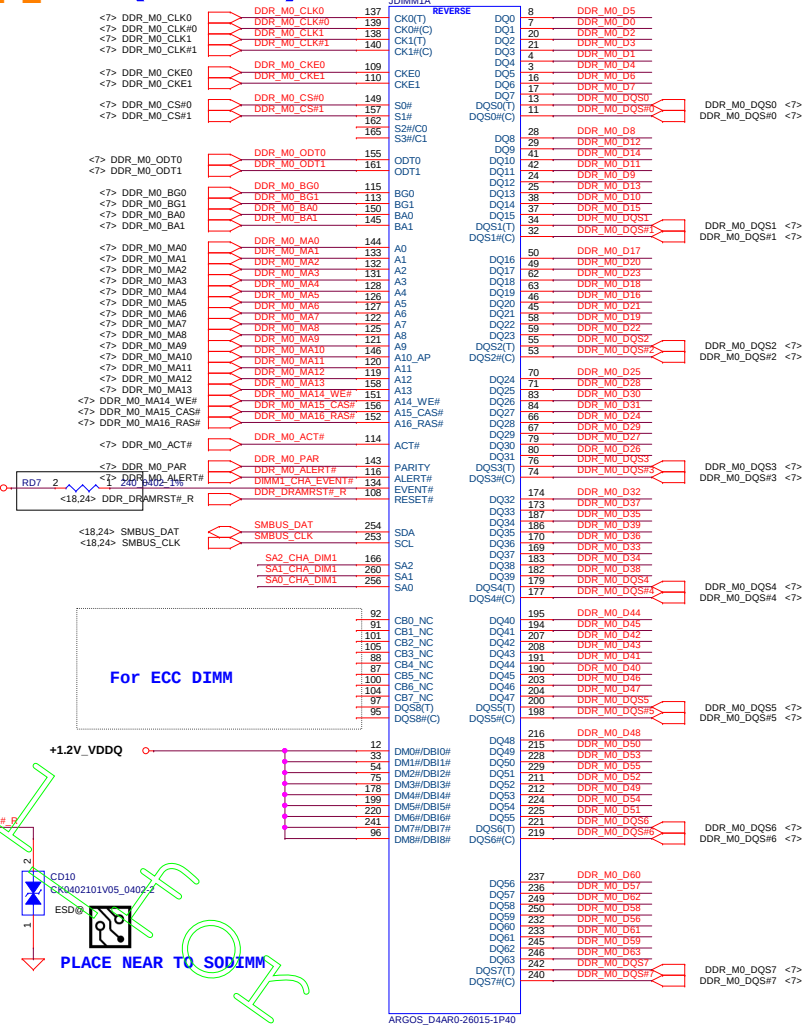


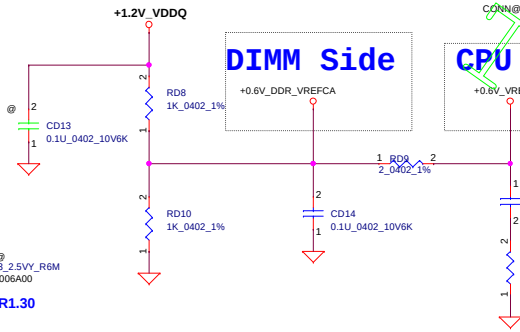












VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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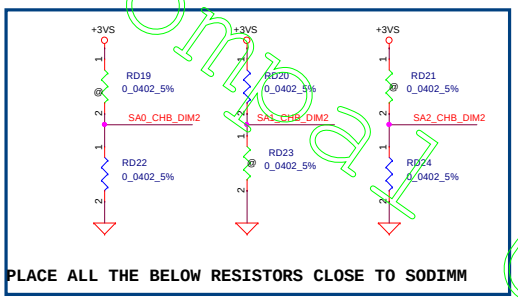
Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Size	Document Number: FPC54 LA-H482P
Rev	v0.1
Date: Friday, September 28, 2018	Sheet 23 of 100

CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

17.3"=>Reverse TYPE (8 mm)

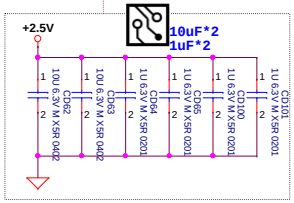
Interleaved Memory



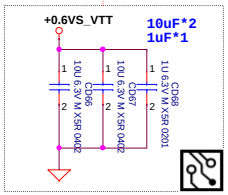
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

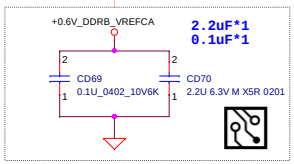
Layout Note:
Place near JDIMM2.257,259



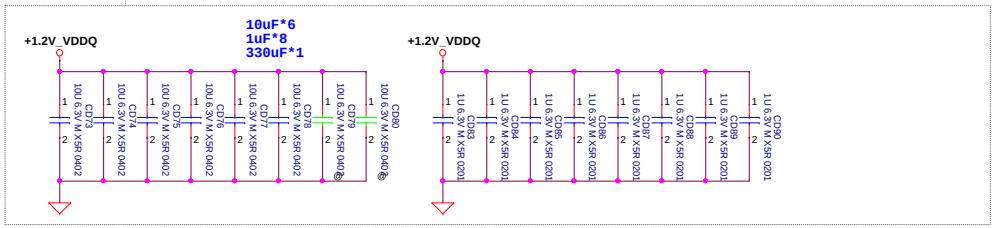
Layout Note:
Place near JDIMM2.258

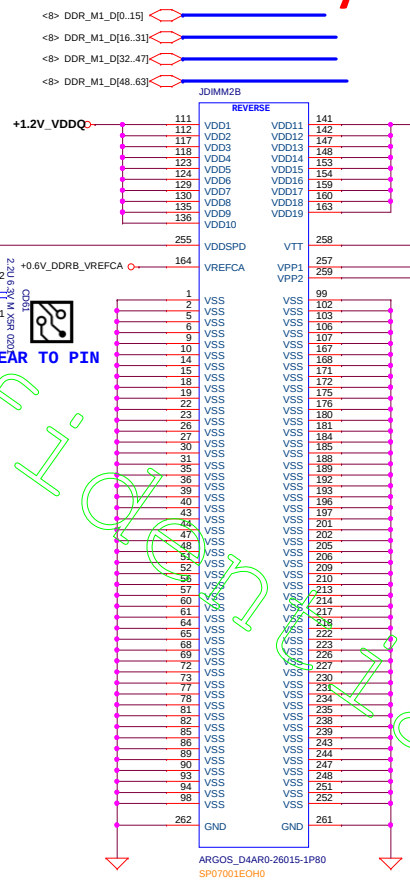


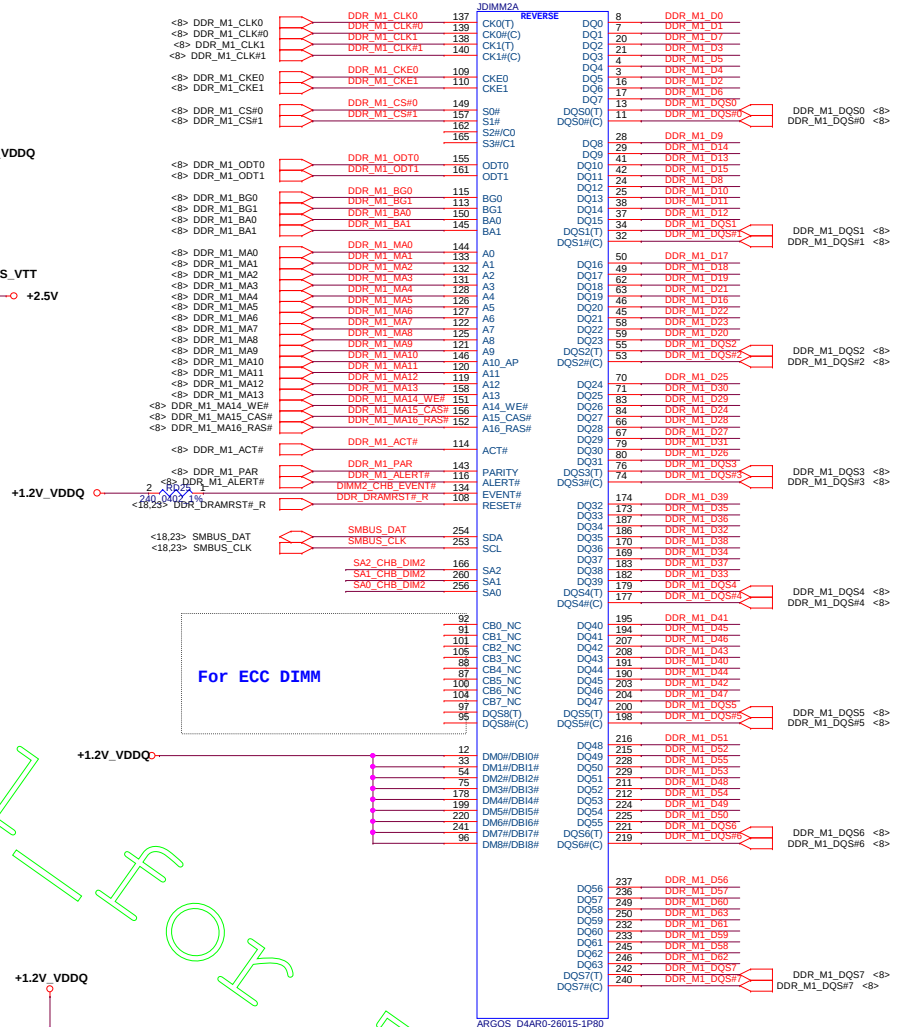
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

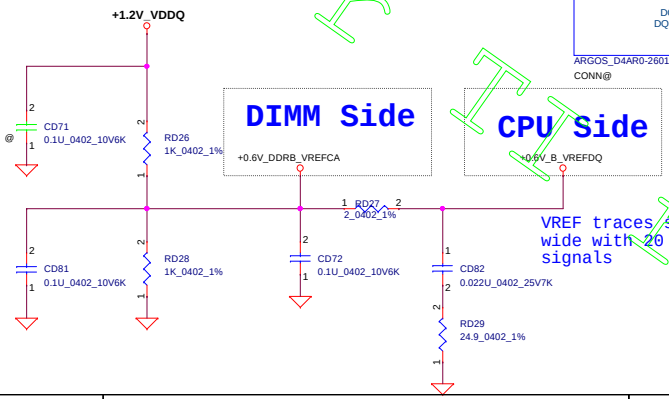


Layout Note:
Place near JDIMM2









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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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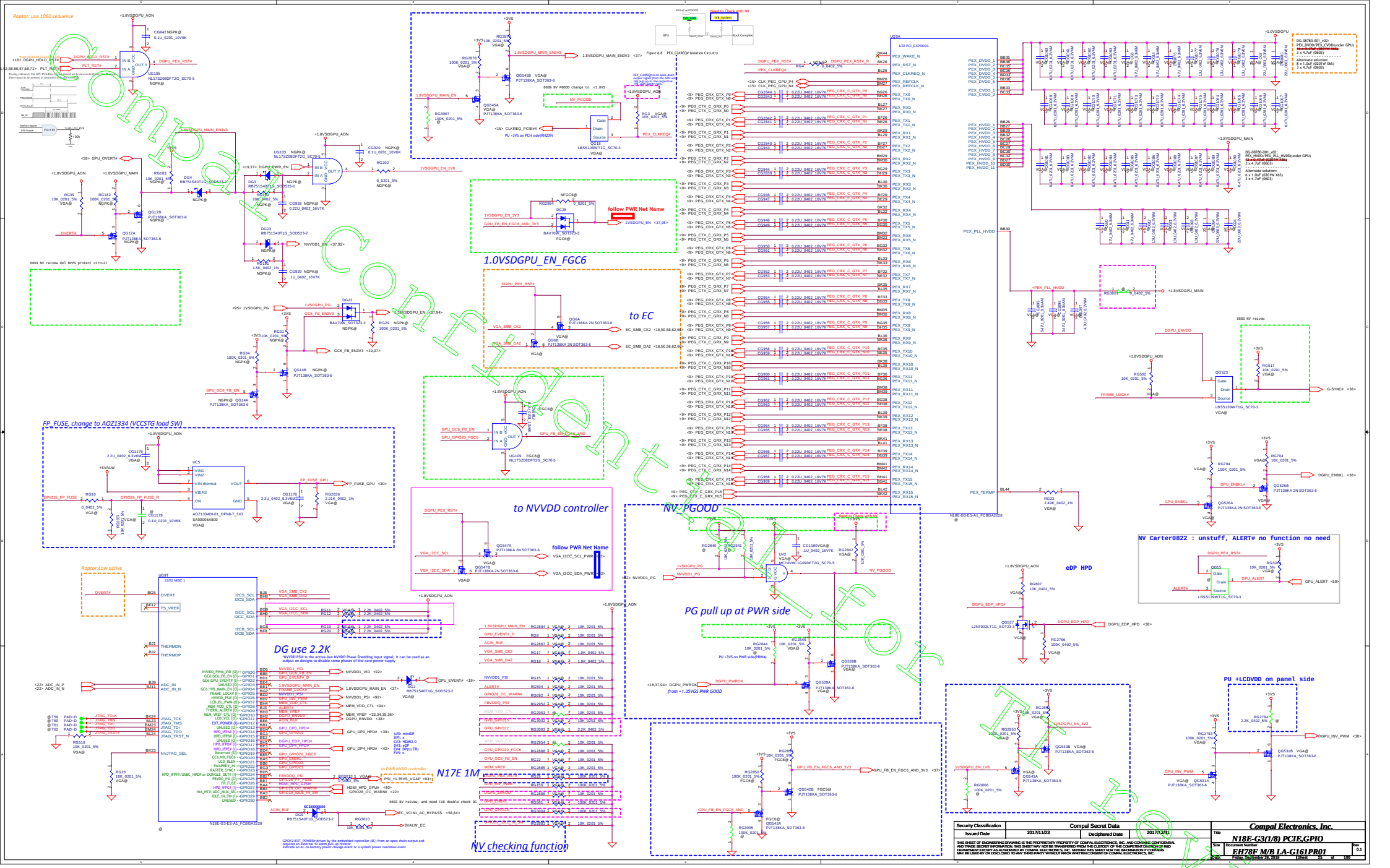
Compal Electronics, Inc.	
Title	DDRIV_CHB: DIMM0
Size	Document Number: FPC72 LA-H492P
Rev	v0.1
Date: Friday, September 28, 2018	Sheet 24 of 100


Raptor: use 1060 sequence
1.0VSDGPU_EN_FGC6
to EC
to NVVDD controller
NV_PGOOD
PG pull up at PWR side
FP_FUSE_change to AOZ1334 (VCCSTG load SW)
DG use 2.2K
N17E 1M
NV checking function
eDP HPD
PU +LCDVDD on panel side
NV Carter0822 : unstuff, ALERT# no function no need
follow PWR Net Name
Raptor:Low active
N18E-G3-ES-A1_FCBGA2228
Compal Electronics, Inc.
N18E-G3(1/8) PCIE,GPIO
EH78F M/B LA-G161PR01
Compal Secret Data
2017/11/23
2017/12/31
Friday, September 28, 2018

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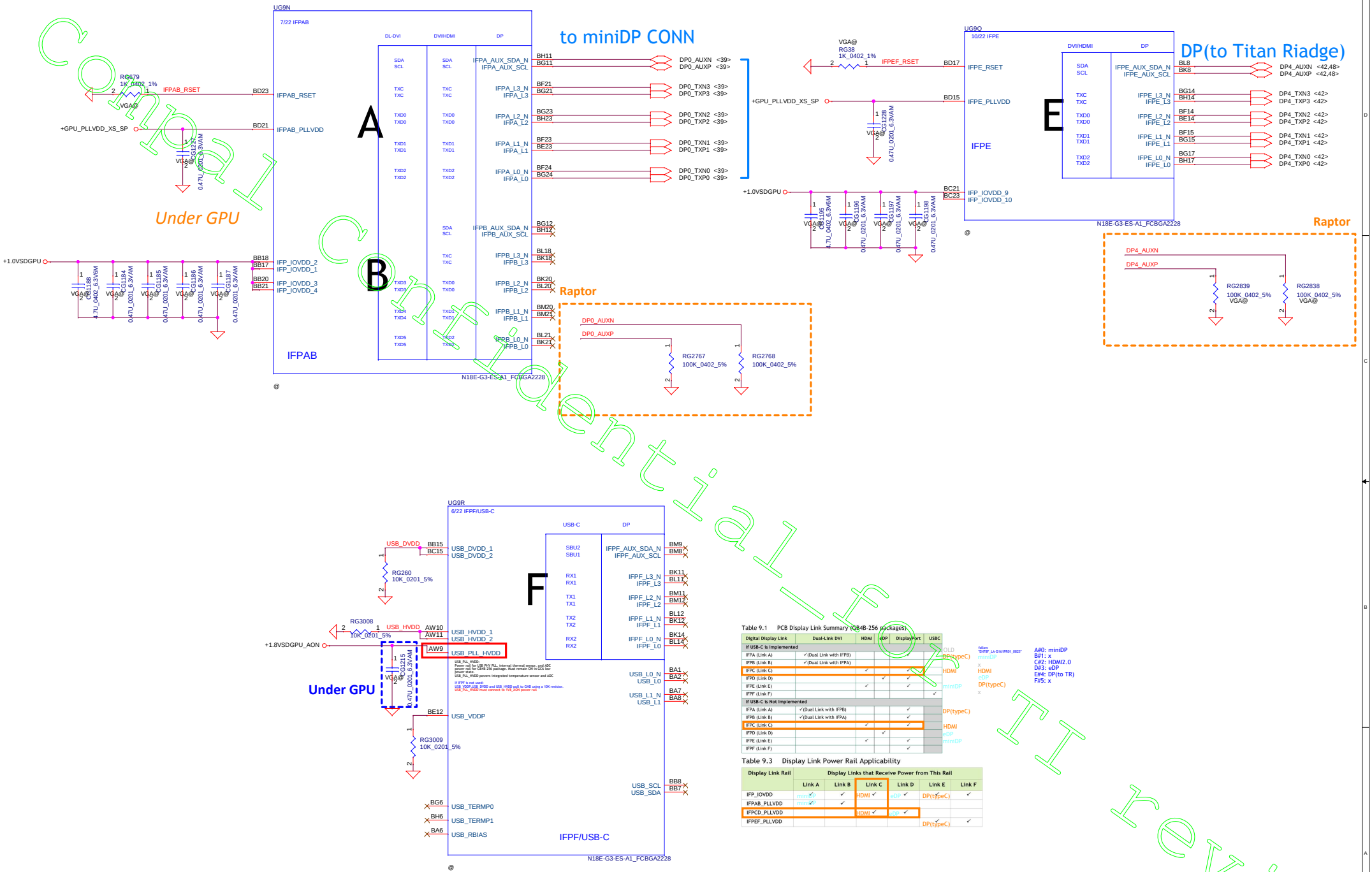

Table 9.1 PCB Display Link Summary (G84B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort	USBC	
If USB-C is Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		HOLD
IFPB (Link B)	✓(Dual Link with IFPA)			✓		DP(typeC)
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓	✓		eDP
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)				✓		
If USB-C is Not Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		DP(typeC)
IFPB (Link B)	✓(Dual Link with IFPA)			✓		
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓			eDP
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)				✓		

follow "EHTYP_LA-G161PR01_0825"

miniDP
x
HDMI
eDP
DP(typeC)
x

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

Table 9.3 Display Link Power Rail Applicability

Display Link Rail	Display Links that Receive Power from This Rail					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	miniDP ✓	✓	HDMI ✓	eDP ✓	DP(typeC) ✓	✓
IFPAB_PLLVDD	miniDP ✓	✓				
IFPCD_PLLVDD			HDMI ✓	eDP ✓		
IFPEF_PLLVDD					DP(typeC) ✓	✓

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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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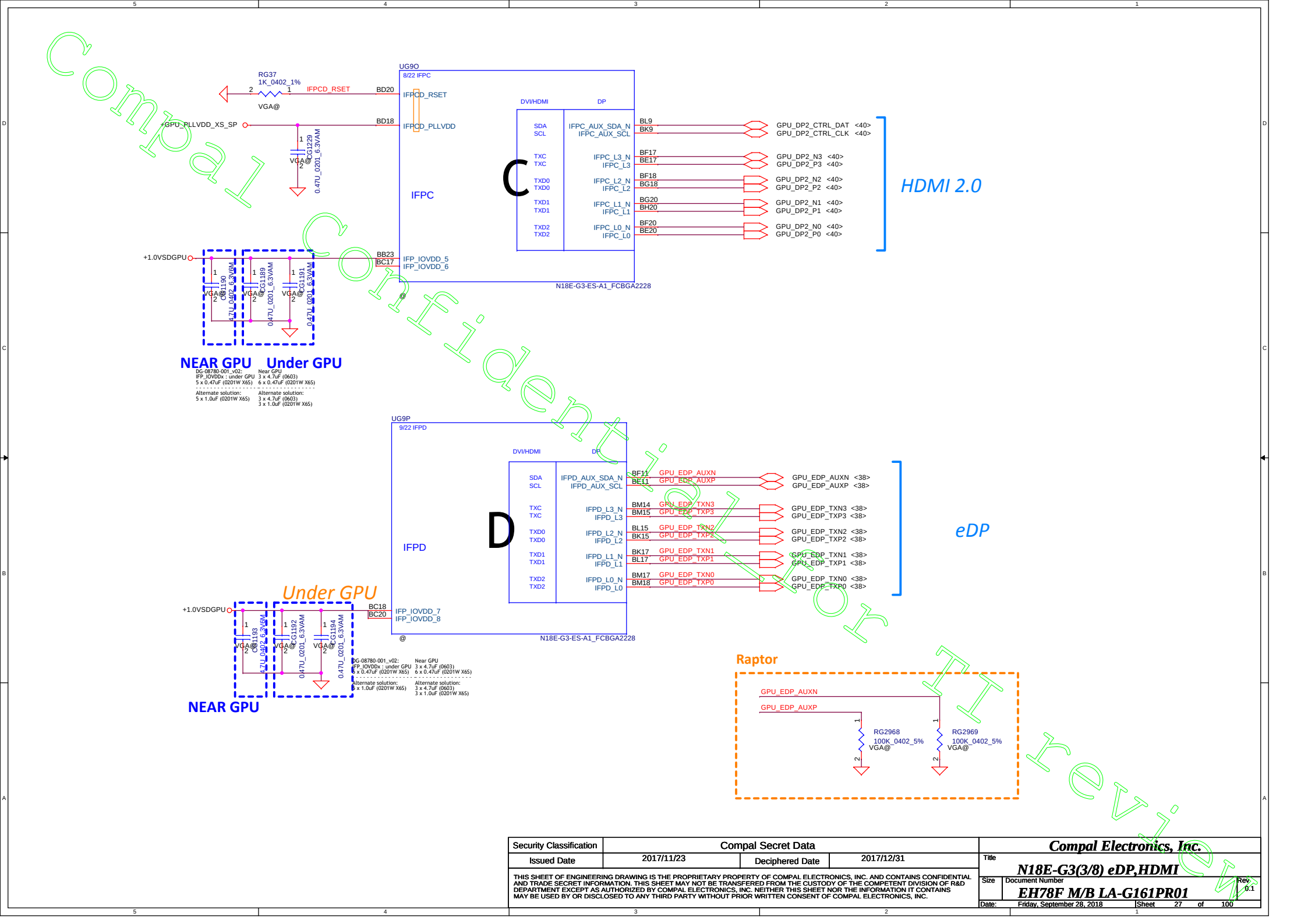
Compal Electronics, Inc.			
Title	N18E-G3(2/8) DP		
Size	Document Number		Rev
	EH78F M/B LA-G161PR01		0.1
Date:	Friday, September 28, 2018	Sheet	26 of 100



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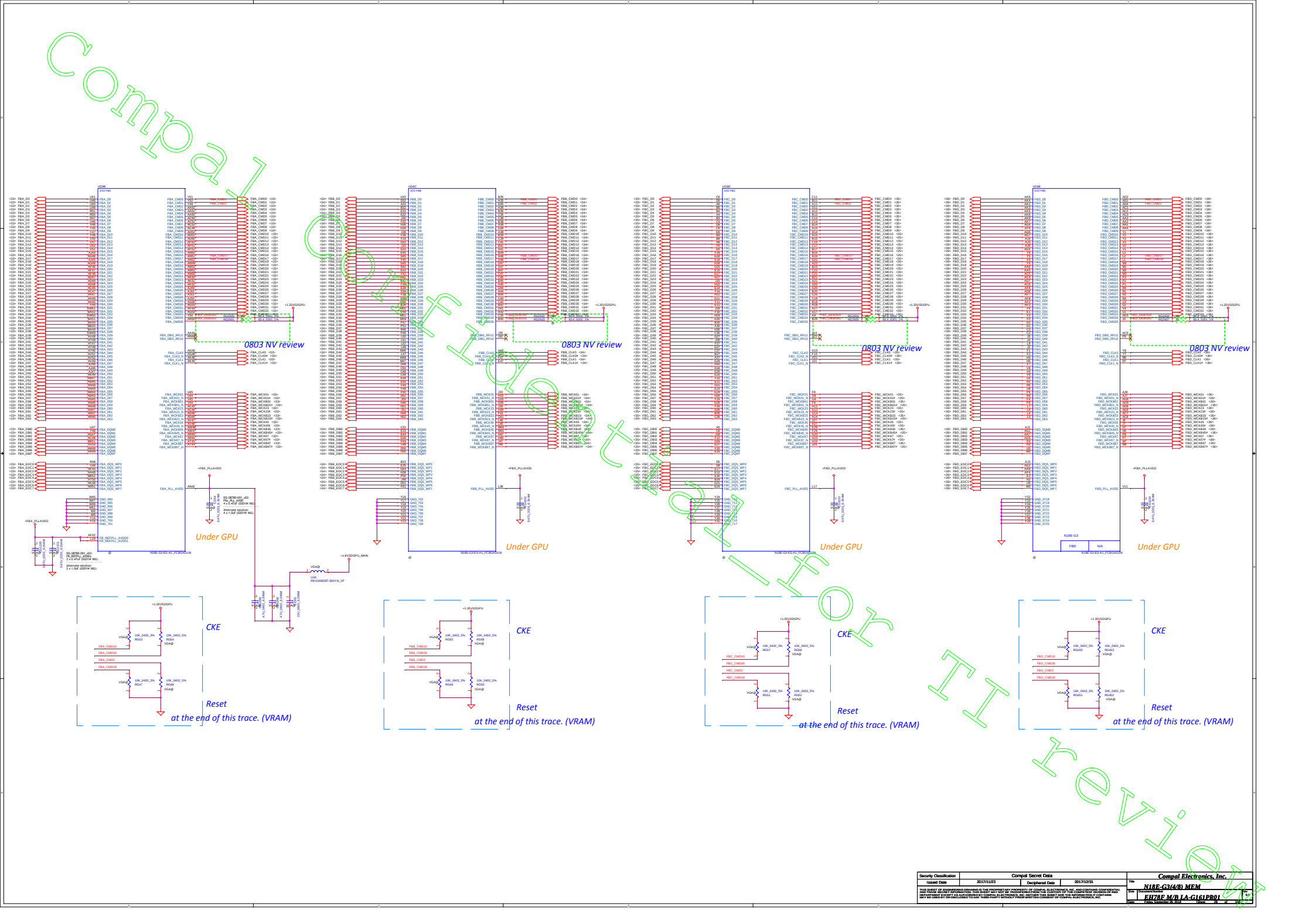
Compal Electronics, Inc.

Title: **N18E-G3(3/8) eDP,HDMI**

Size: | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 27 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/11/23	Deciphered Date	2017/12/31
Title	N18E-G3(4/8) MEM		
Size	Document Number		Rev
	EH78F M/B LA-G161PR01		0.3
Date:	Tuesday, December 26, 2017	Sheet 39 of 46	

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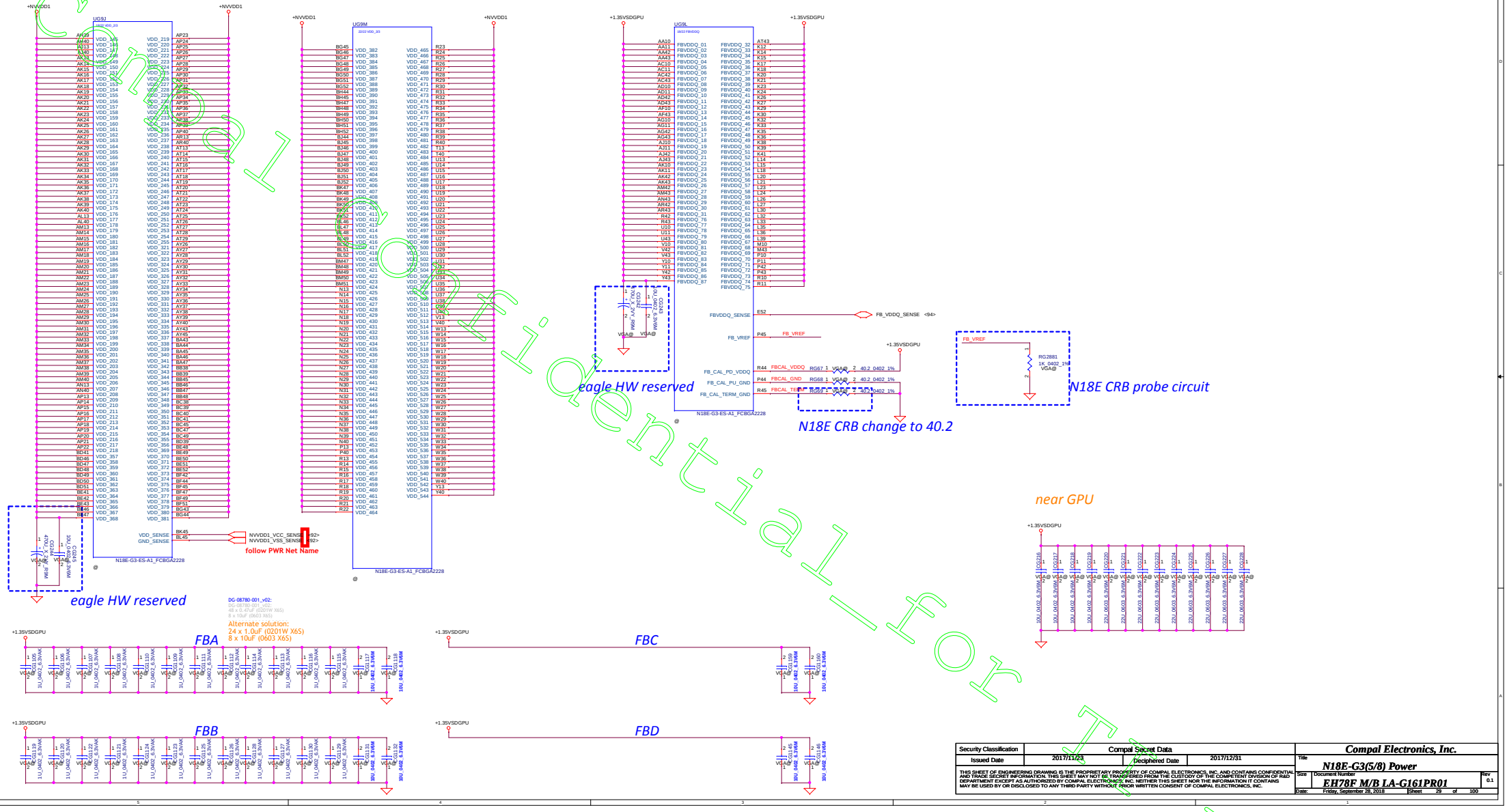

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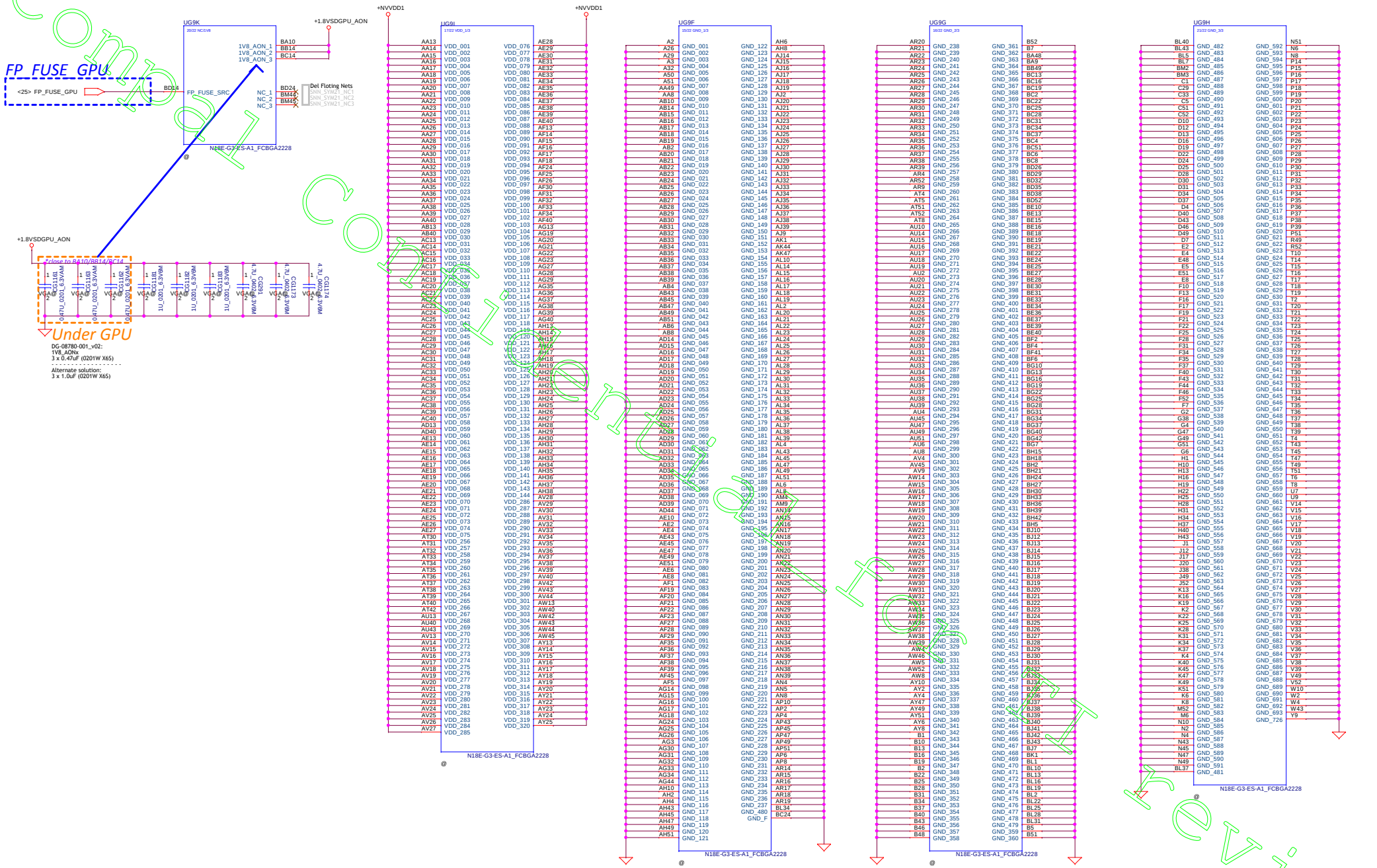
Compal Electronics, Inc.	
Title	N18E-G3(5/8) Power
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date: Friday, September 28, 2018	Sheet 29 of 100


FP_FUSE_GPU
<25> FP_FUSE_GPU
BD14
FP_FUSE_SRC
UG9K
20/22 NC/SVB
1V8_AON_1
1V8_AON_2
1V8_AON_3
BA10
BB14
BC14
+1.8VSDGPU_AON
BD24
BM44
BM45
NC_1
NC_2
NC_3
Del Floting Nets
SNN_SYM21_NC1
SNN_SYM21_NC2
SNN_SYM21_NC3
N18E-G3-ES-A1_FCBGA2228
+NVVDD1
UG9I
17/22 VDD_1/3
UG9F
15/22 GND_1/3
UG9G
16/22 GND_2/3
UG9H
21/22 GND_3/3
Close to B10/B814/BC14
CG1101
CG1102
CG1103
CG1104
CG1105
CG1106
CG1107
CG1108
CG1109
CG1110
CG1111
CG1112
CG1113
CG1114
CG1115
CG1116
CG1117
CG1118
CG1119
CG1120
CG1121
CG1122
CG1123
CG1124
CG1125
CG1126
CG1127
CG1128
CG1129
CG1130
CG1131
CG1132
CG1133
CG1134
CG1135
CG1136
CG1137
CG1138
CG1139
CG1140

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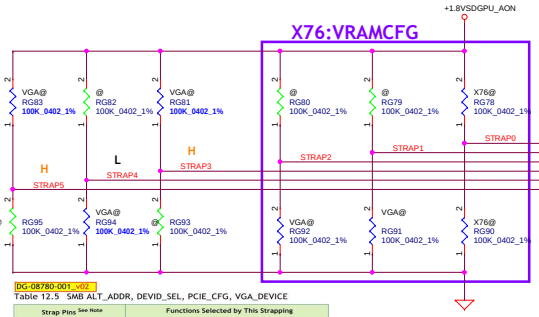
X76:VRAMCFG



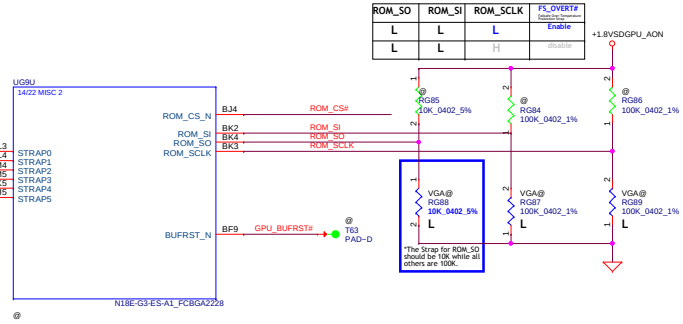
DG-08780-001_v02

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

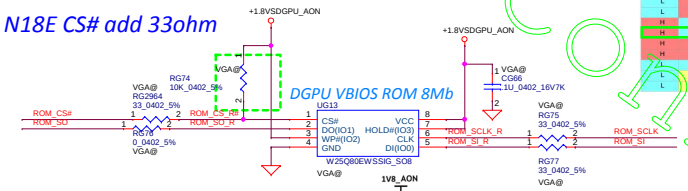
DEVID_SEL:
0: Normal Panel
1:G-SYNC Panel

VGA_DEVICE:
0: No Display out
1:GPU Display out=1



ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT#
L	L	L	Enable
L	L	H	disable

N18E CS# add 33ohm



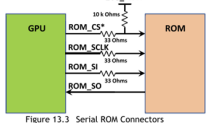
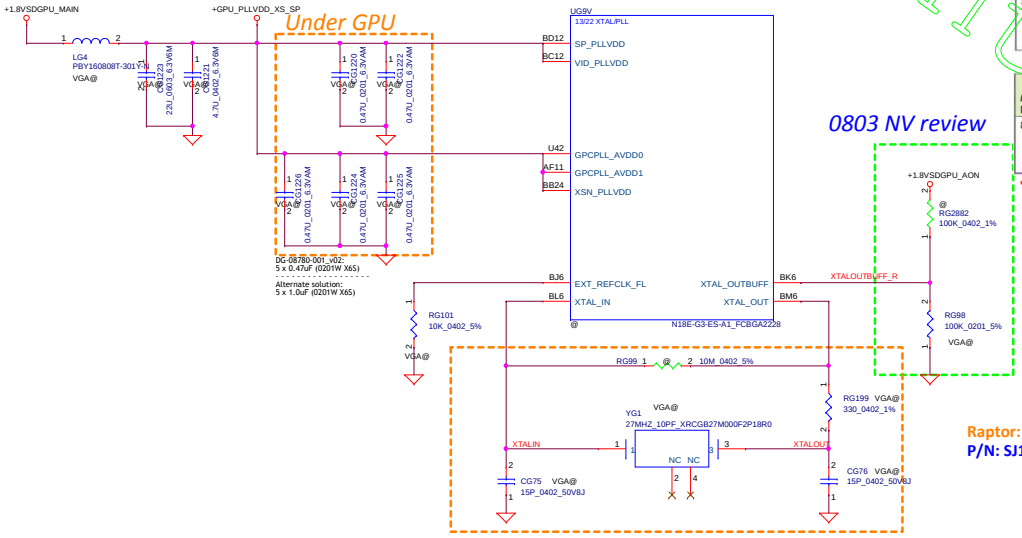


Figure 13.3 Serial ROM Connectors

Under GPU



0803 NV review

RVL-08928-001_v03	N18E G3	N18E G2	N18E G1	(MSB) Strap2	Strap1	(LSB) Strap0	(MSB) Strap5	Strap4	(LSB) Strap3	ROM_SO	ROM_SI	ROM_SCLK	Note
Micron MT61K256M32JE-14:A (0x1)	V	V	TBD	PD 100kOhm	PD 100kOhm	PU 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Samsung K4Z80325BC-HC14 (0x0)	V	V	TBD	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Hynix H56C8H24MJR-S2C (0x2)		V	TBD	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
TBD													

Note: GPU Discrete or Hybrid impact Strap3~Strap5 deisgn

RVL-08928-001_v04

Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 3. N18E-G0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

*DVS is required. WCK: TBD

Table 12.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	M	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Raptor: change to follow 2018 VX SJ10000UI00
P/N: SJ10000UI00 (S CRYSTAL 27MHZ 10PF XRCGB27M000F2P18R0)

vinafix

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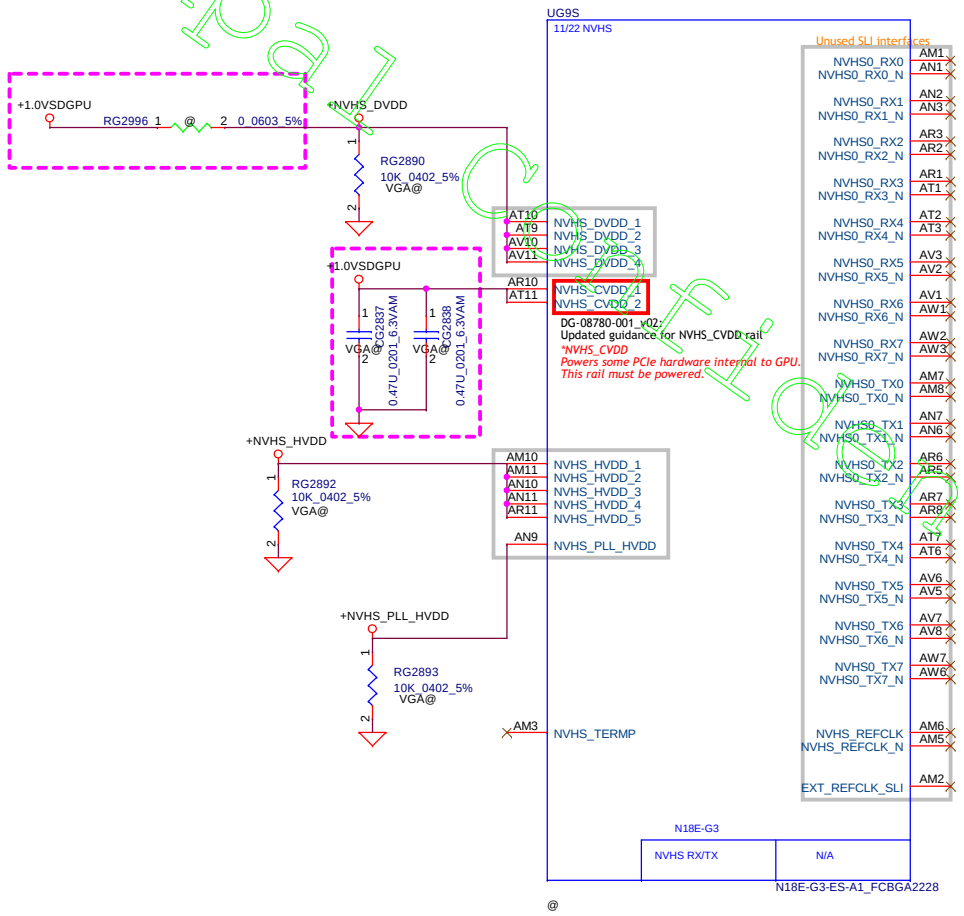
Compal Electronics, Inc.

Title: N18E-G3(7/8) Strap,ROM

Size: | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 31 of 100

Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



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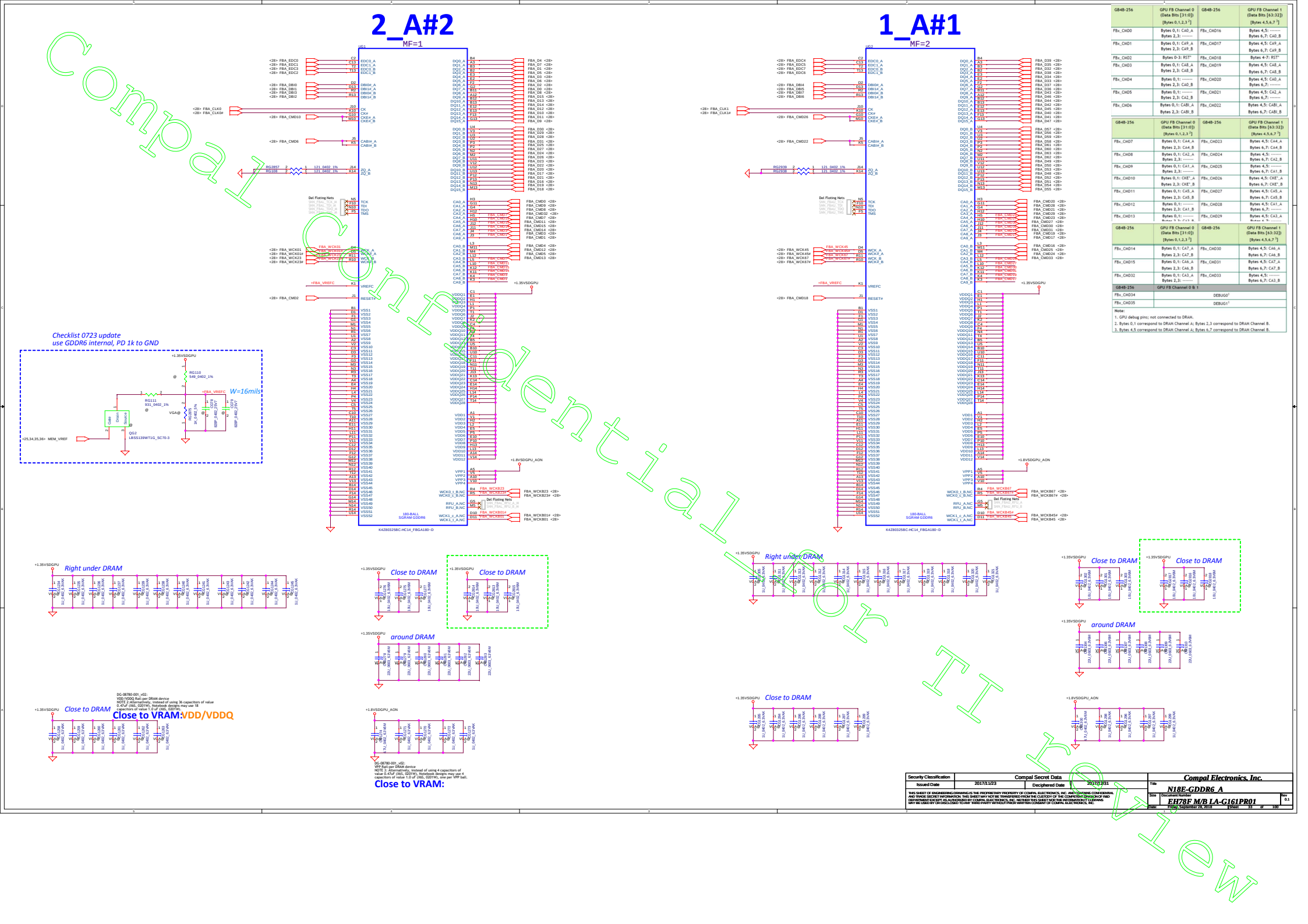
Compal Electronics, Inc.

Title: **N18E-G3(8/8) NVLINK**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 32 of 100



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: --------	FBx_CMD16	Bytes 4,5: -------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Byte 0-3: RST#	FBx_CMD18	Bytes 4-7: RST#
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: -------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: --------
FBx_CMD5	Bytes 0,1: -------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: --------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: --------	FBx_CMD24	Bytes 4,5: -------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: --------	FBx_CMD25	Bytes 4,5: -------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE'_A Bytes 2,3: CKE'_B	FBx_CMD26	Bytes 4,5: CKE'_A Bytes 6,7: CKE'_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: -------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: --------
FBx_CMD13	Bytes 0,1: -------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: --------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: --------	FBx_CMD33	Bytes 4,5: -------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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4_B#2

MF=1

3_B#1

MF=2

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Checklist 0723 update
use GDDR6 internal PD 1k to GND

W=16mils

Right under DRAM

Close to DRAM

around DRAM

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6_C#2

MF=1

5_C#1

MF=2

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE*_A Bytes 2,3: CKE*_B	FBx_CMD26	Bytes 4,5: CKE*_A Bytes 6,7: CKE*_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Checklist 0723 update
use GDDR6 internal, PD 1k to GND

Right under DRAM

Close to DRAM

around DRAM

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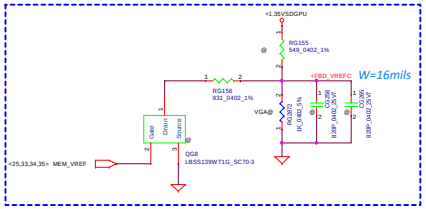
MF=1

# 7_D#1
MF=2



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: ------	FBx_CMD16	Bytes 4, 5: ------ Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------ Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: ------
FBx_CMD5	Bytes 0, 1: ------ Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: ------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: ------	FBx_CMD24	Bytes 4, 5: ------ Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: ------	FBx_CMD25	Bytes 4, 5: ------ Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------ Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: ------
FBx_CMD13	Bytes 0, 1: ------ Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: ------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: ------	FBx_CMD33	Bytes 4, 5: ------ Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Right under DRAM
Close to DRAM
around DRAM

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Issued Date	2017/11/23	Deciphered Date	2017/12/31
			Title: N18E-GDDR6_D
			Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1
			Date: Friday, September 28, 2018 Sheet 35 of 105

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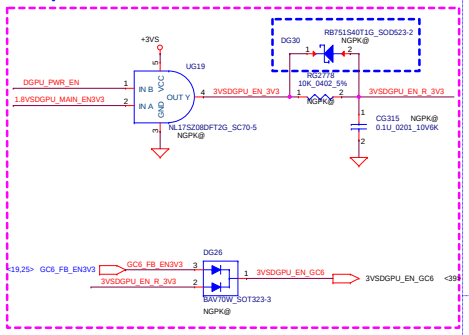
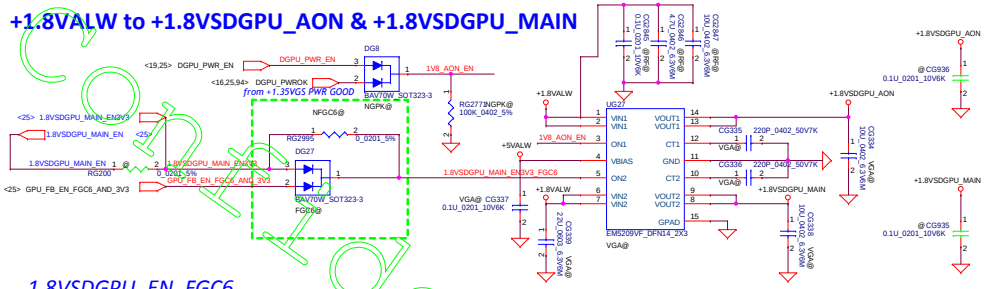
No Reserved NV Sequence IC: SILEGO GreenPAK
SA0000B9H00, S IC SLG4U41989VTR STQFN 20P LOGIC SOC

+3VS/+3VSDGPU

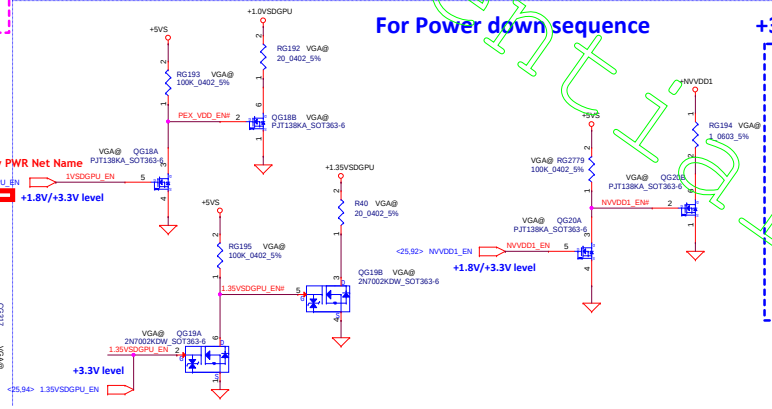


+1.8VALW to +1.8VSDGPU_AON & +1.8VSDGPU_MAIN

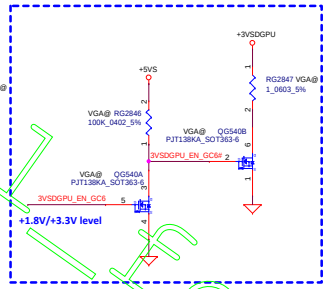


1.8VSDGPU_EN_FGC6

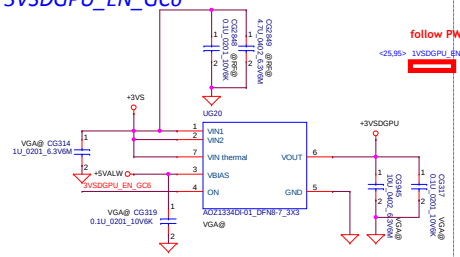
For Power down sequence



+3VSD_GPU discharge if need

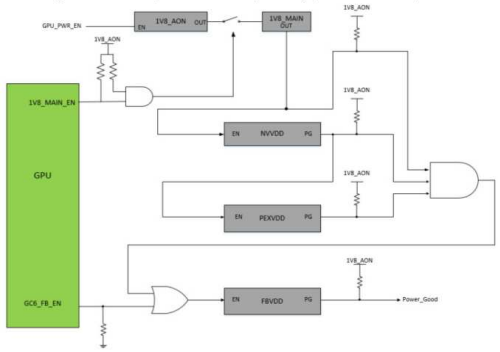


3VSDGPU_EN_GC6

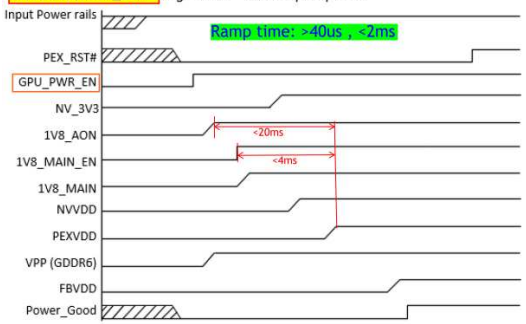


DG-08780-001_v02

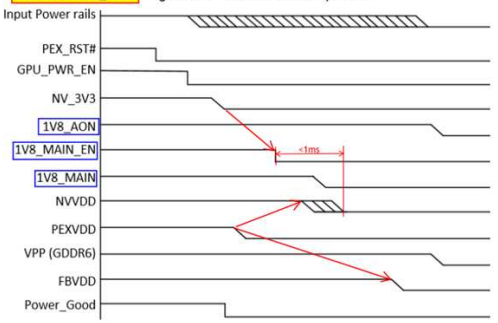
Figure 5.5 Example of Power Sequencing (GPU rails shown)



DG-08780-001_v02 Figure 5.6 Power-Up Sequence



DG-08780-001_v02 Figure 5.7 Power-Down Sequence



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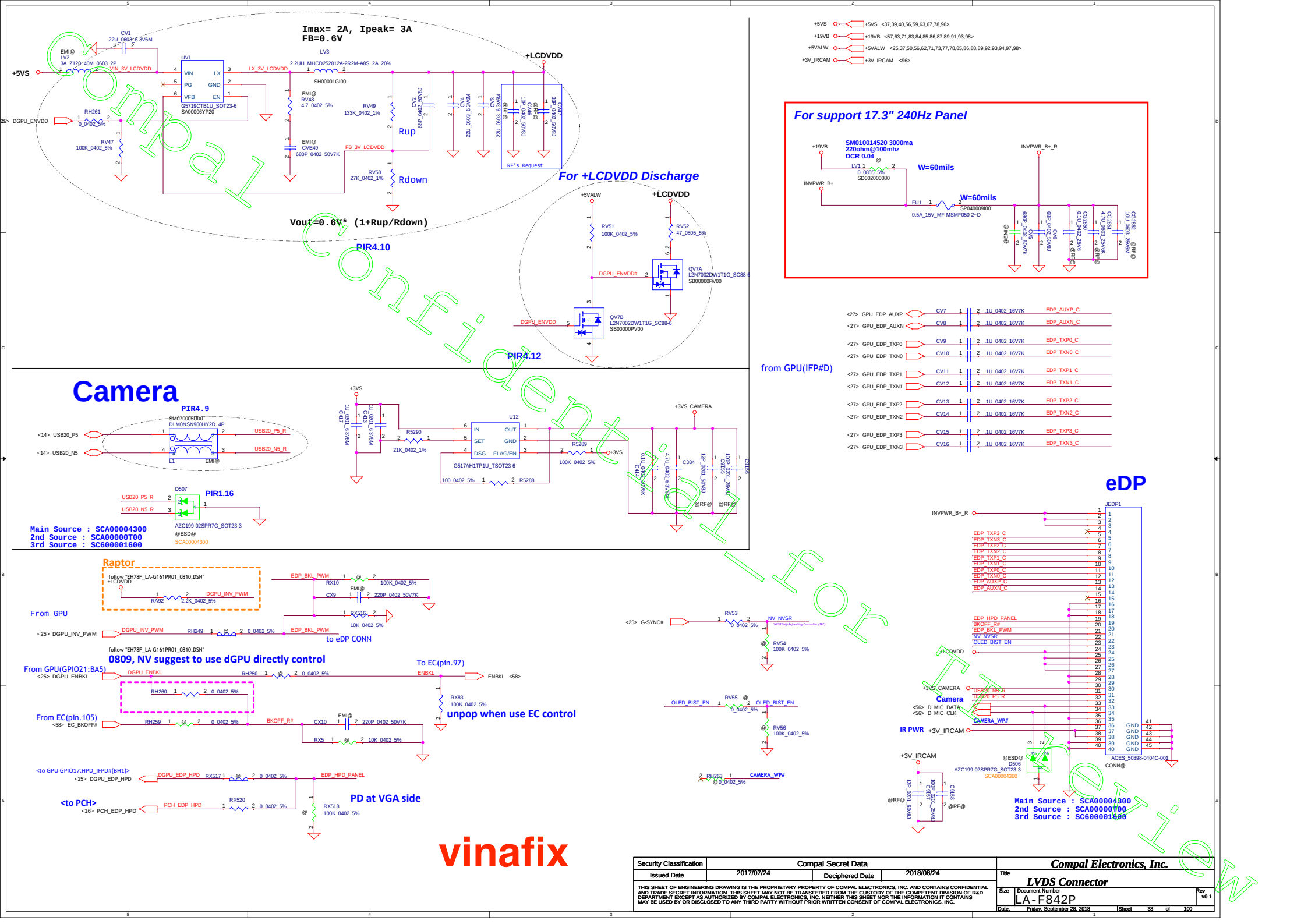
Compal Electronics, Inc.	
Title	N18E-GPU Power control
Size / Document Number	EH78F M/B LA-G161PR01
Rev	0.1
Date: Friday, September 28, 2018	Sheet 37 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24
Title	LVDS Connector		
Size	Document Number		Rev
	LA-F842P		v0.1
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0 = GPIO mode (I2C disabled)

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

bit[2]H:1 / bit[1]L:0

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

DP only

Need Check

Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SCG00001600

DP++ and isolated circuit

minDP HPD

OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1 (0:DP)
L	H	B2	A=B2 (1:HDMI)
H	X	Z	NC

W=40mils W=40mils

0921 change souce to +3VALW, CTRL to SUSP#

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Issued Date	2017/11/23	Deciphered Date	2018/09/01

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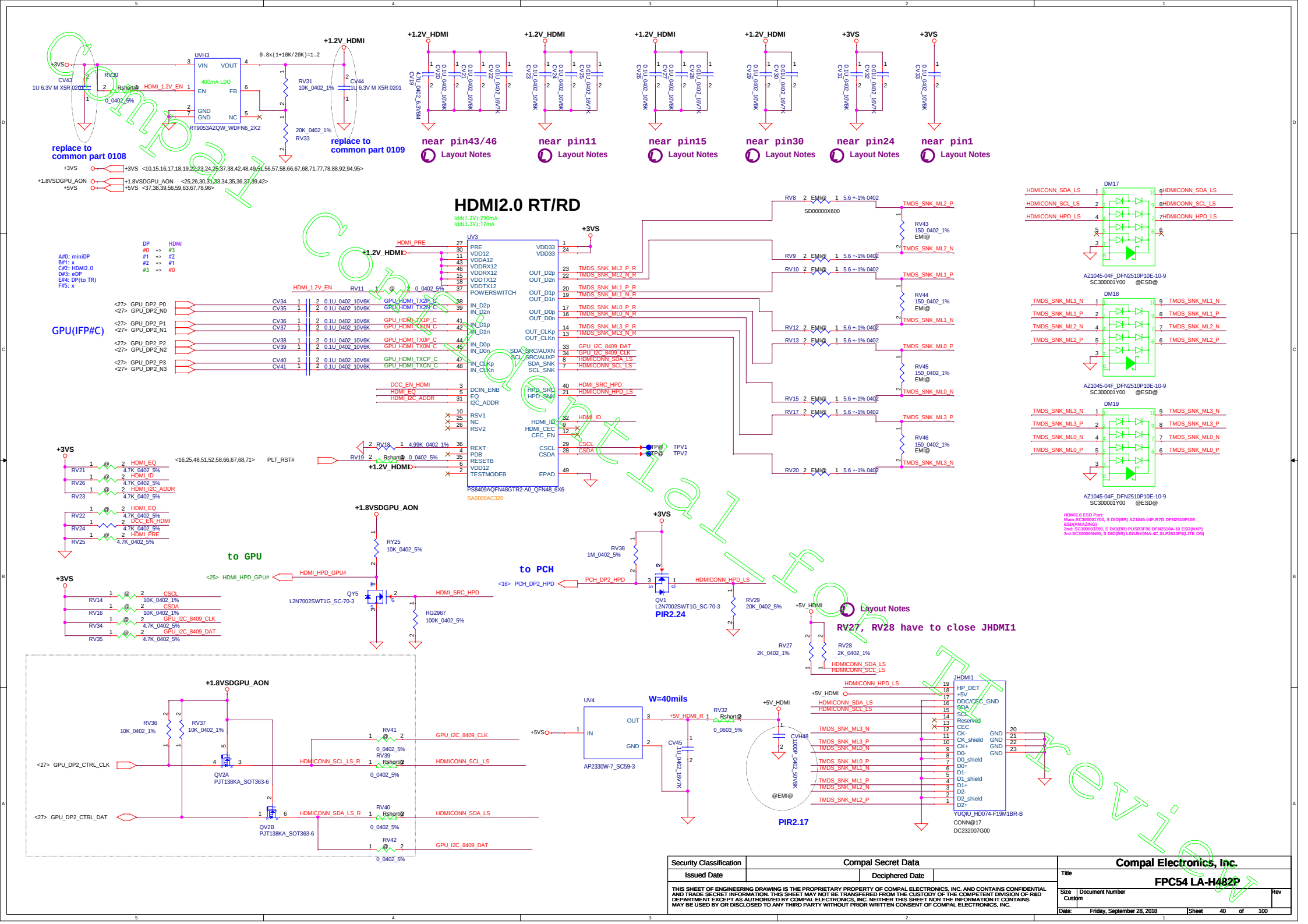
Compal Electronics, Inc.

Title: mDP redriver(TUSB546)

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 39 of 100


HDMI2.0 RT/RD
UV3
PS8409AQFN48GTR2-A0_QFN48_6X6
SA0000AC320
UVH3
RT9053AZQW_WDFN6_2X2
UV4
AP2330W-7_SC59-3
QV1
L2N7002SWT1G_SC-70-3
QV2A
QV2B
PJT138KA_SOT363-6
QY5
JHDMI1
YUQIU_HD074-F19M1BR-B
CONN@17
DC232007G00
DM17
DM18
DM19
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00 @ESD@
GPU(IFP#C)
to GPU
to PCH
PIR2.24
PIR2.17
W=40mils
RV27, RV28 have to close JHDMI1
replace to common part 0108
replace to common part 0109
near pin43/46
near pin11
near pin15
near pin30
near pin24
near pin1
Layout Notes
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1012 check Ti if need

+3VS
LT39
+3V_TYPEC_DP
PBY160808T-600Y-N_2P
TBT@
+3VS
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,48,49,51,56,57,58,66,67,68,71,77,78,88,92,94,95>

0 = GPIO mode (I2C disabled)

I2C_EN_TBT — RT8441 2 1K_0402_5% — +3V_TYPEC_DP
RT8461 2 1K_0402_5% — TBT@

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

CTL1_TBT_HPDIN — bit[2]H:1 — RT8431 2 1K_0402_5% — +3V_TYPEC_DP
RT8451 2 1K_0402_5% — TBT@

CTL0_TBT_SDA — bit[1]L:0 — RT9001 2 1K_0402_5% — +3V_TYPEC_DP
RT8471 2 1K_0402_5% — TBT@

FLIP_TBT_CLK — bit[1]L:0 — RT8481 2 1K_0402_5% — +3V_TYPEC_DP
RT8491 2 1K_0402_5% — TBT@

DPEQ0_A1_TBT — RT8501 2 1K_0402_5% — +3V_TYPEC_DP
RT8511 2 1K_0402_5% — TBT@

DPEQ1_TBT — RT8521 2 1K_0402_5% — +3V_TYPEC_DP
RT8531 2 1K_0402_5% — TBT@

DPEQ0,DPEQ1 : DP Receiver equalization gain F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

A0_TBT — RT8541 2 1K_0402_5% — +3V_TYPEC_DP
RT8551 2 1K_0402_5%

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

Copy from "EH78F_LA-G161PR01_0810_P.42"

Simplified Schematics

+3V_TYPEC_DP
CT305 1 2 10U_0402_6.3V6M TBT@
CT306 1 2 1U_0201_6.3V6K @
CT307 1 2 0.1U_0201_10V6K TBT@
CT320 1 2 0.1U_0201_10V6K TBT@
CT308 1 2 0.1U_0201_10V6K TBT@
CT309 1 2 0.1U_0201_10V6K TBT@

UT11 660mW : 4 Lane DP Only at 8.1Gbps
CTL1 = H; CTL0 = L
TUSB546_QFN40_4X6 TBT@

VCC (1, 6, 20, 28)
I2C_EN
DPEQ1 / DPEQ0/A1
SSEQ1 / SSEQ0/A0
FLIP/SCL
CTL0/SDA
CTL1
SCTXp / SCTXn
RESVD1 →CAD_SNK
RESVD2 →HPDIN
PAD

from GPU(IFP#E)

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

<26> DP4_TXP0 / <26> DP4_TXN0 — CT310 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP0_C — CT311 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN0_C — DP0p / DP0n
<26> DP4_TXP1 / <26> DP4_TXN1 — CT312 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP1_C — CT313 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN1_C — DP1p / DP1n
<26> DP4_TXP2 / <26> DP4_TXN2 — CT314 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP2_C — CT315 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN2_C — DP2p / DP2n
<26> DP4_TXP3 / <26> DP4_TXN3 — CT316 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP3_C — CT317 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN3_C — DP3p / DP3n

DP only — Set to "4 Lane DP-No Flip"

<48> TRP_N3 / <48> TRP_P3 — RX1n / RX1p
<48> TRP_N0 / <48> TRP_P0 — RX2n / RX2p

DP only

TBT@ +3V_TYPEC_DP RT856 1 2 4.7K_0402_5%
@ RT857 1 2 4.7K_0402_5%
<16,48> TBT_DP0_HPD — RT858 1 2 0_0402_5% TBT@ — TBT_DP0_HPD_R

+1.8VSDGPU_AON
R810 10K_0402_5% TBT@
<25> GPU_DP4_HPD#
A#0: miniDP / B#1: x / C#2: HDMI2.0 / D#3: eDP / E#4: DP(to TR) / F#5: x
QV97 L2N7002LT1G_SOT23-3 TBT@
TBT_DP0_HPD
R397 100K_0402_5% TBT@

to TR sink port#1

TH41 TP@ / TH40 TP@
I2C_EN_TBT
DPEQ1_TBT / DPEQ0_A1_TBT
TH42 TP@ — A0_TBT
FLIP_TBT_CLK
CTL0_TBT_SDA
CTL1_TBT_HPDIN

TRP_N2 <48> / TRP_P2 <48>
TRP_P1 <48> / TRP_N1 <48>

TH43 TP@ / TH44 TP@

TBT@ RD_DP4_AUXP_C — 0.1U_0201_10V6K — CT318 — DP4_AUXP <26,48>
RD_DP4_AUXN_C — 0.1U_0201_10V6K — CT319 — DP4_AUXN <26,48>

+3V_TYPEC_DP
RT859 100K_0402_5% TBT@
RD_DP4_AUXN_C
RD_DP4_AUXP_C
RT860 100K_0402_5% TBT@

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Title: TBT DP redriver

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 42 of 100

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Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 47 of 100		

Copy from "DDX03_LS-F262PR02_0309A"

Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

"559414-manufacturing-test-thunderbolt-mas-rev-2-3-from-9-21-2017"
CNL supports HBR3 (8.1G), but no DSC (so only DP1.3), DP1.4 supported in TR, but only via discrete GFX silicon w/ DP1.4 logic

Titan Ridge
Dual Port(TR-DP): JHL7540
Single Port(TR-SP):JHL7340

+3VALW <14,18,20,39,49,50,51,52,58,63,66,71,78,85,86,87,91,92,94,95>
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,49,51,56,57,58,66,67,68,71,77,78,88,92,94,95>
+3V_TBT_LC <49>

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From SoC PCIe TX

PCIe_IN#0

PCIe GEN3

To SoC PCIe RX

PCIE RBIAS
Place as close as possible to pins

GPU(IFP#E)+Repeater TUSB546
From dGPU DDIx4 for DPv1.4

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

DP_IN#1

DP_IN#2

DP_OUT#0

SINK PORT 1

SINK PORT 2

SOURCE PORT 0

LC GPIO

POC GPIO

MISC

USB

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled
DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

Follow TR_DP_TI_PD_HOST_REF_DESIGN_R0V95
PE isn't POR -
Please don't use

From TPS65987S.

Need Check if 10k?(RT33)

Place as close as possible to pins

Port_OUT#A

Port A

TBT PORTS

PORT B

NC

DEBUG

USB2 Rbias Place as close as possible to pins

Remove JTAG1 Conn

25M XTAL

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

Dead Battery Mode (Default):
To Support Dead Battery mode R5 should be populate.
+3V_TBT_A_LDO should be connected to +3V_Flash
Desktop:
To support Desktop/RVP, R4 should be populate.
+3VALW should be connected to +3V_Flash

Figure 1. Titan Ridge SP Controller Block Diagram

Main Source:SC40000DS00
2nd Source : SC40000AT00
3rd Source : SC40000DM00

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Date: Friday, September 28, 2018	Sheet: 48 of 100		

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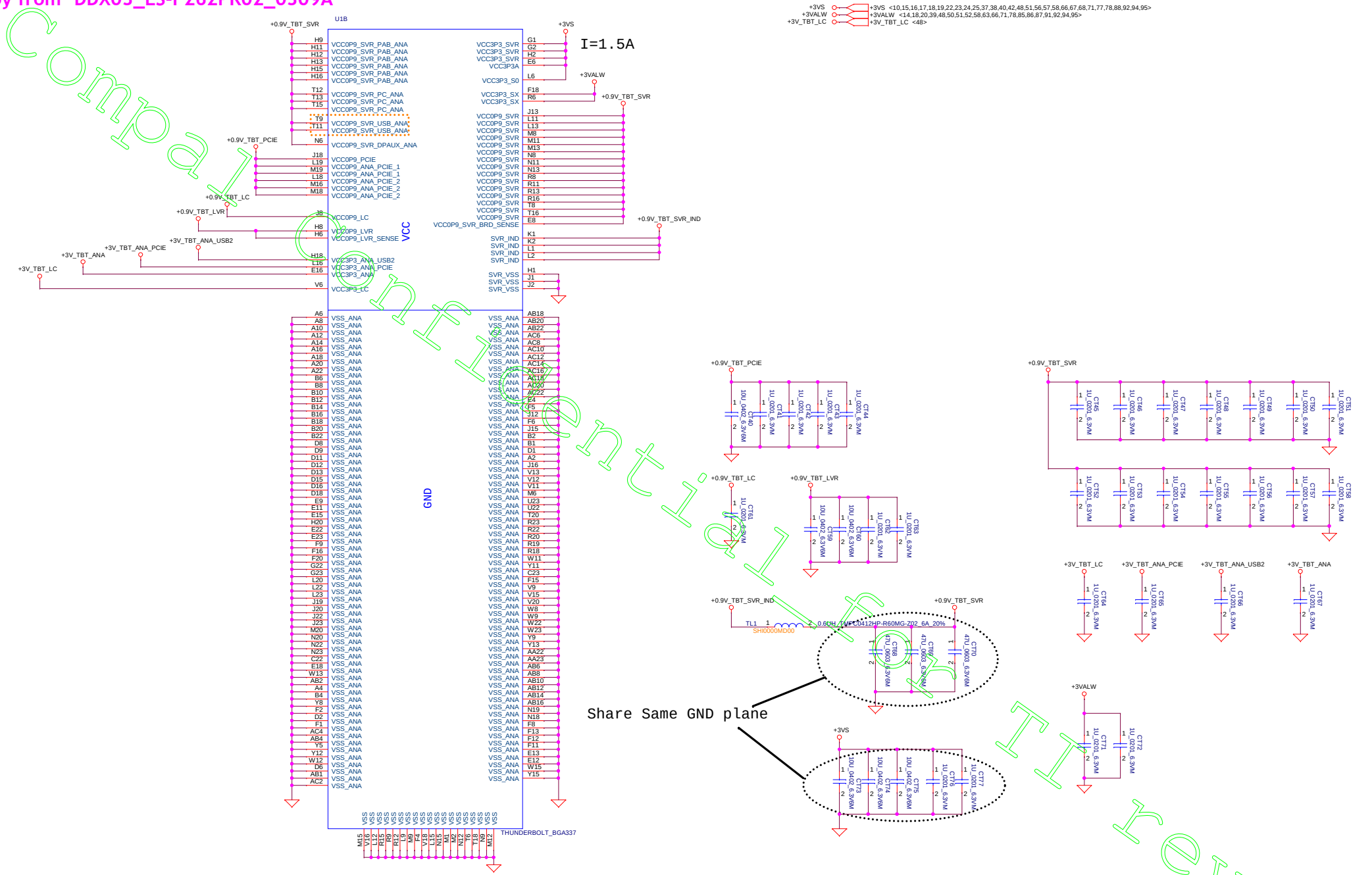

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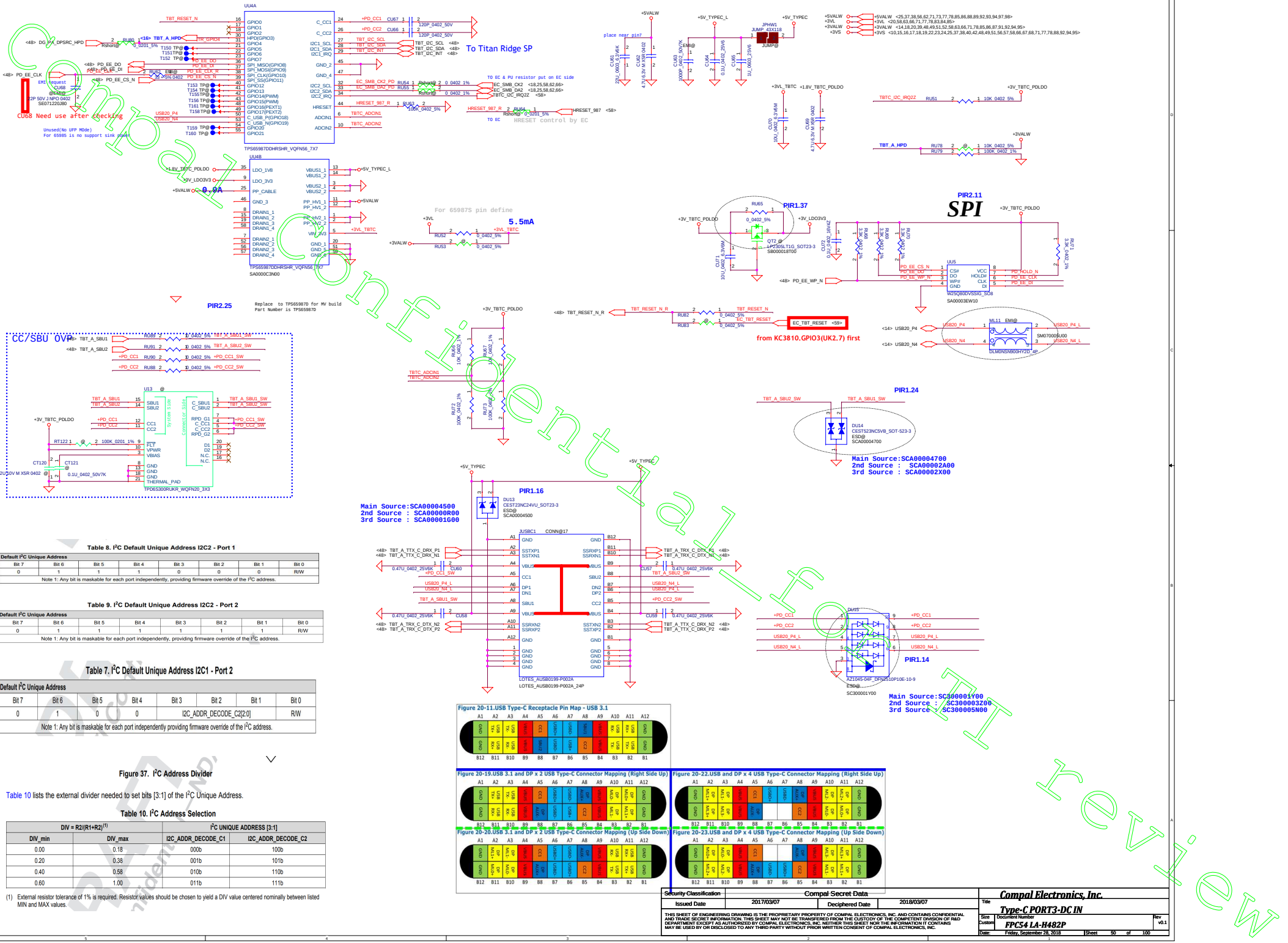

Table 8. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 9. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Figure 20-11.USB Type-C Receptacle Pin Map - USB 3.1

Figure 20-19.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Right Side Up)

Figure 20-22.USB and DP x 4 USB Type-C Connector Mapping (Right Side Up)

Figure 20-20.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Up Side Down)

Figure 20-23.USB and DP x 4 USB Type-C Connector Mapping (Up Side Down)

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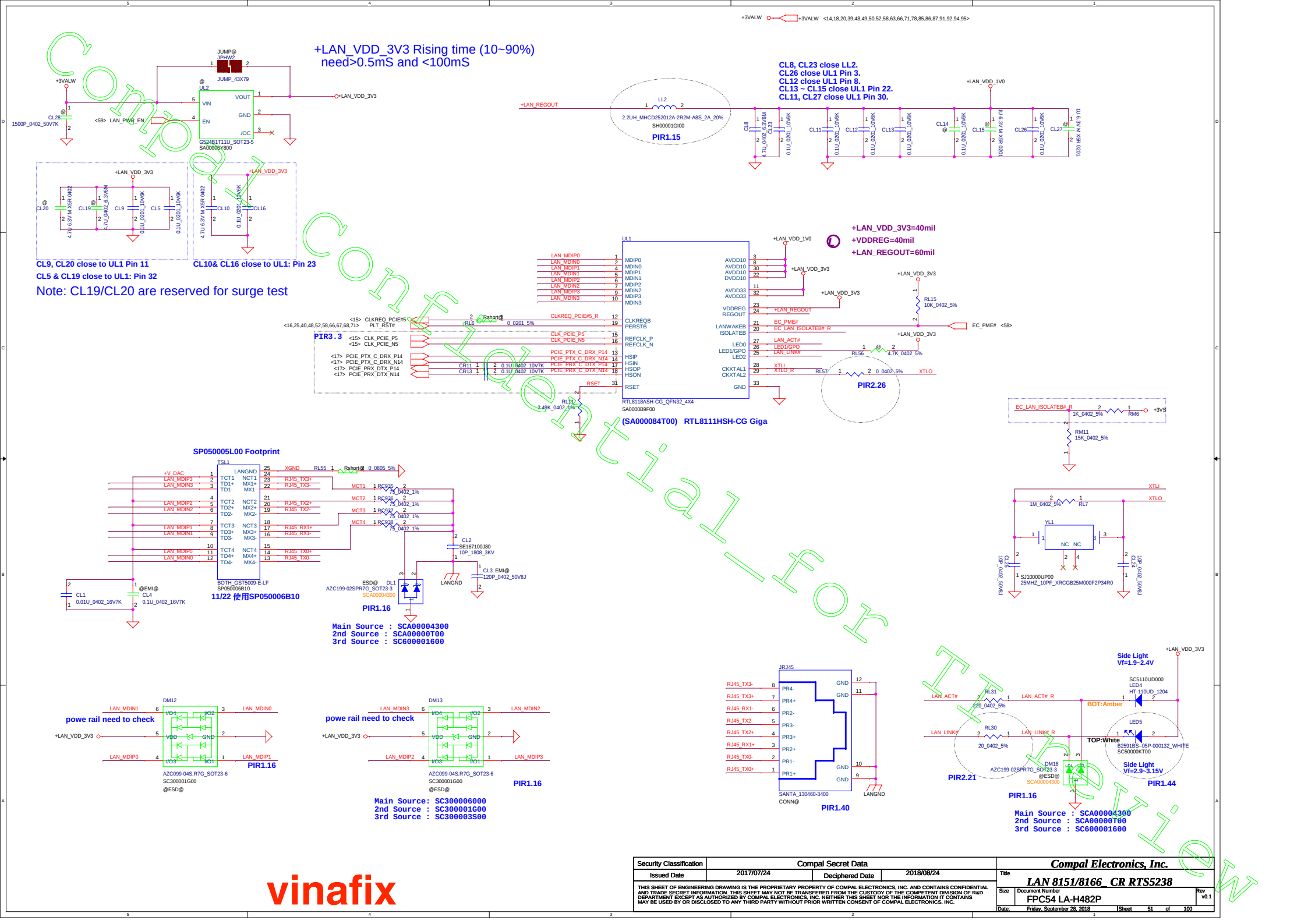

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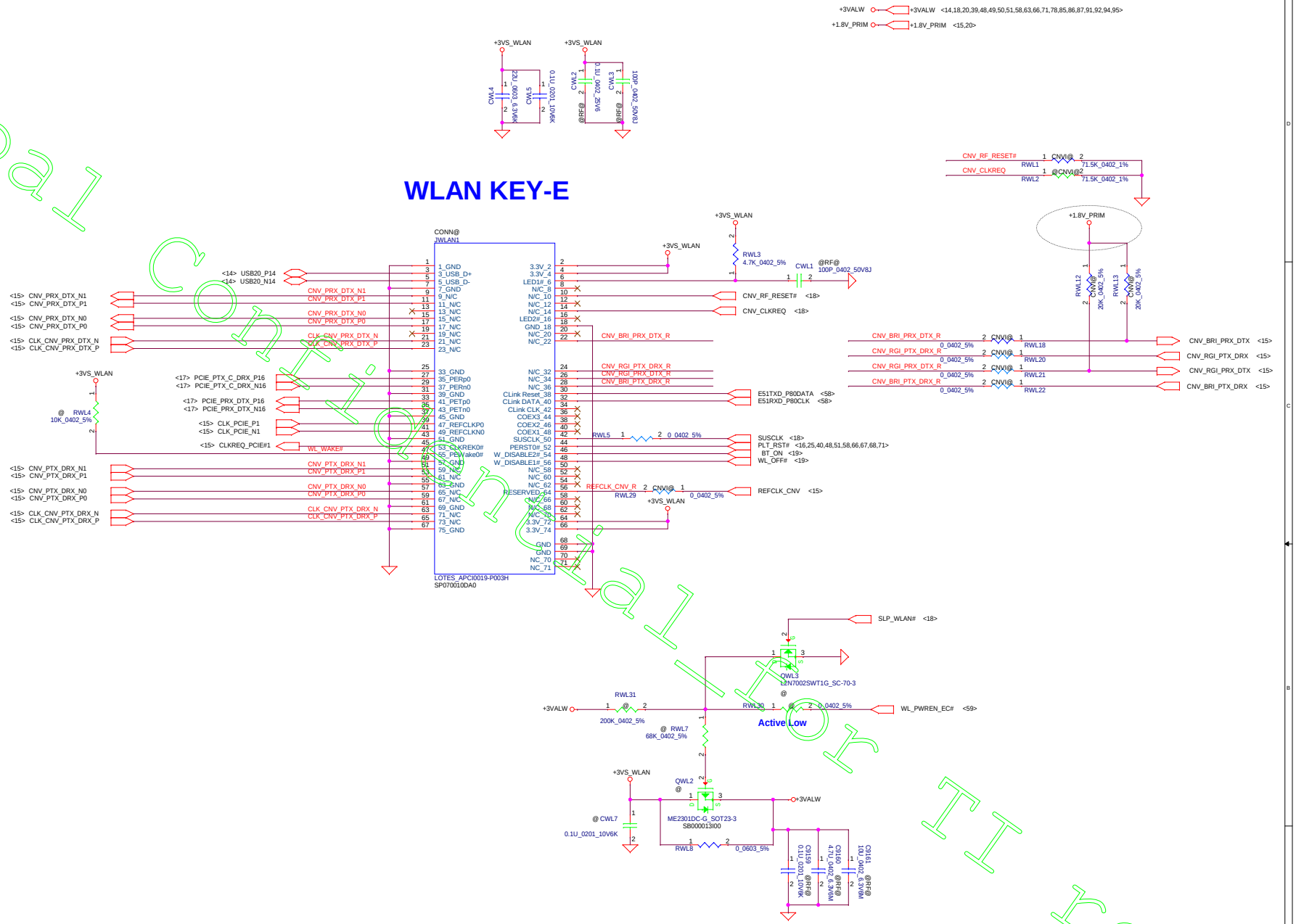
WLAN KEY-E



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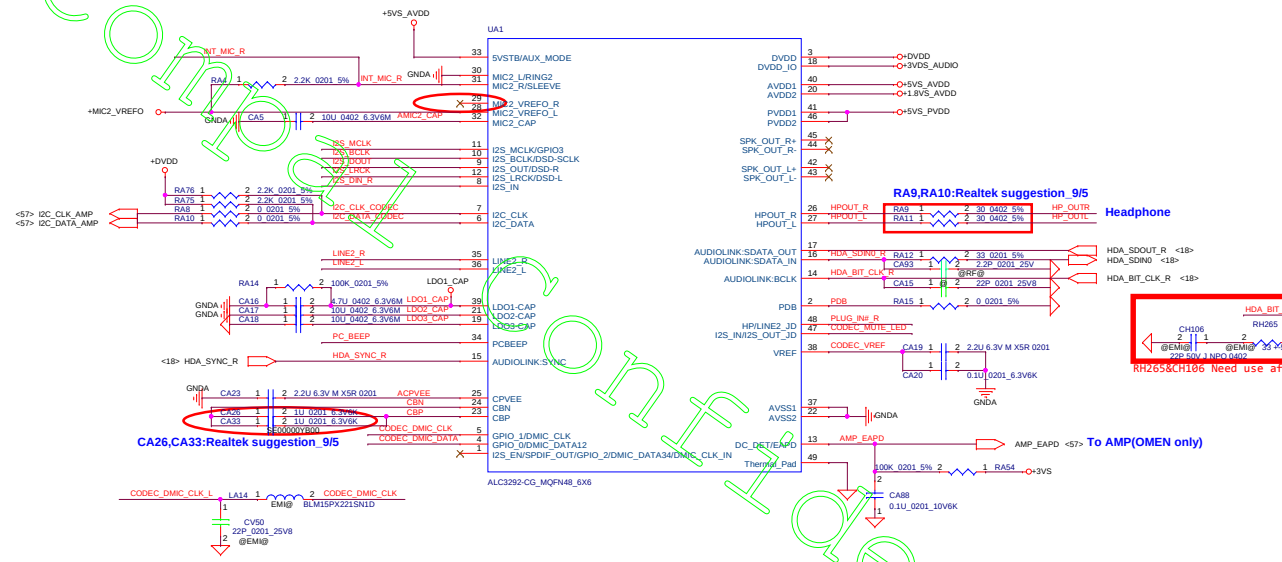
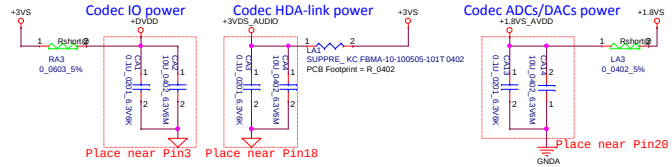
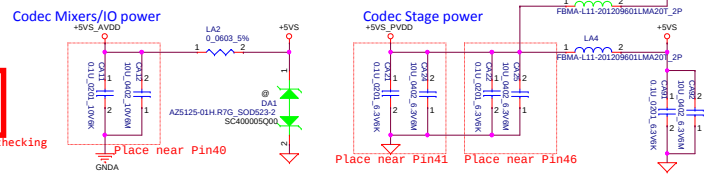
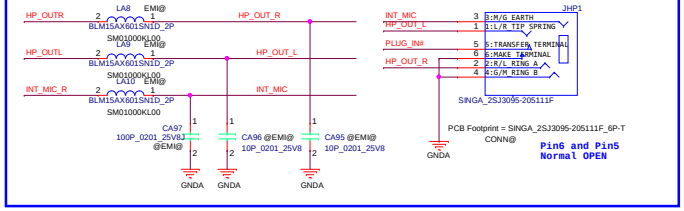


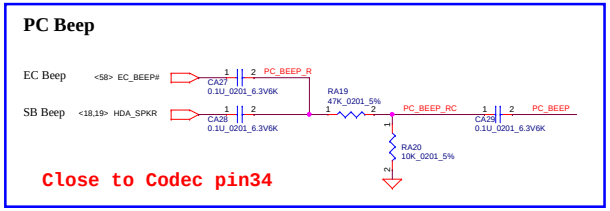




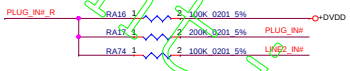
Combo Jack



PC Beep

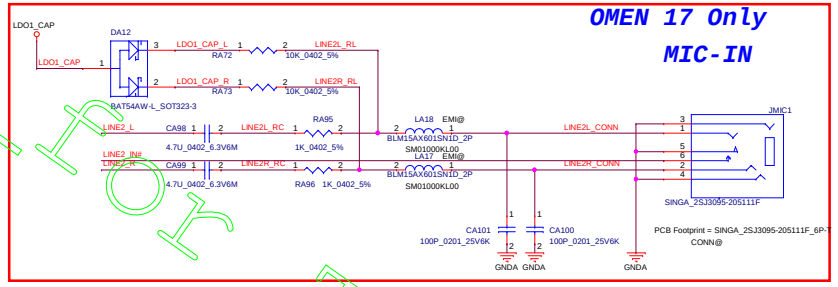


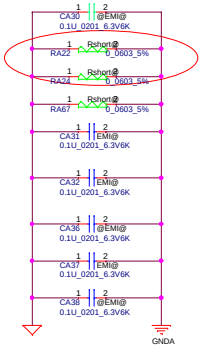
Jack Detect

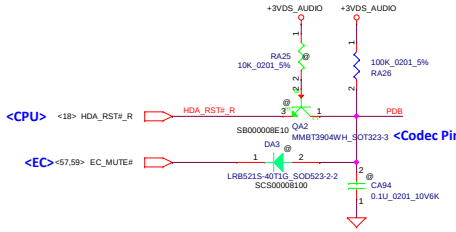


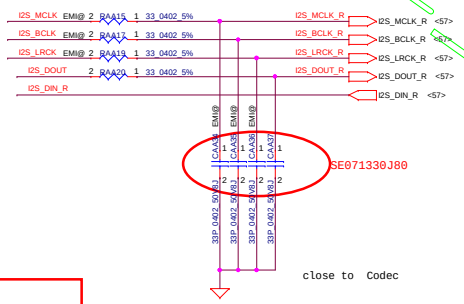
	RA16	RA17	RA74
OMEN_15	@	0_ohm	@
OMEN_17	100K	200K	100K

OMEN 17 Only MIC-IN









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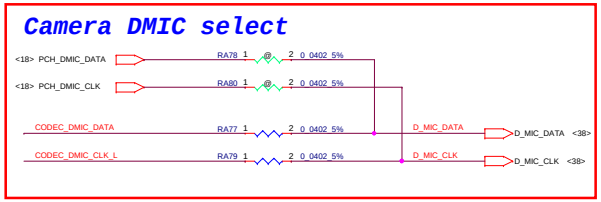
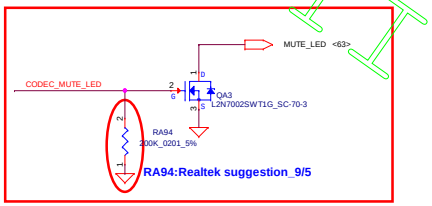
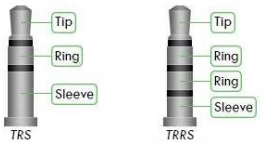






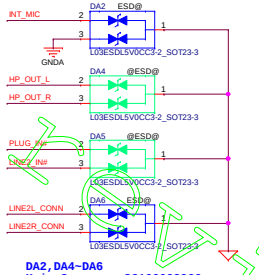
Headphone Jack Type

Audio jack must be plastic without conductive coatings (no chrome)

Individual Audio Jack for Headphone & Microphone

Audio jack pin configuration:
Combo Jack (Headset / Headphone compatible)
Tip = Left
1st ring = Right
2nd ring = Ground
Sleeve = Mono microphone

Microphone Jack (Milos/Santorini Only)
Tip = Left
Ring = Right
Sleeve = Ground



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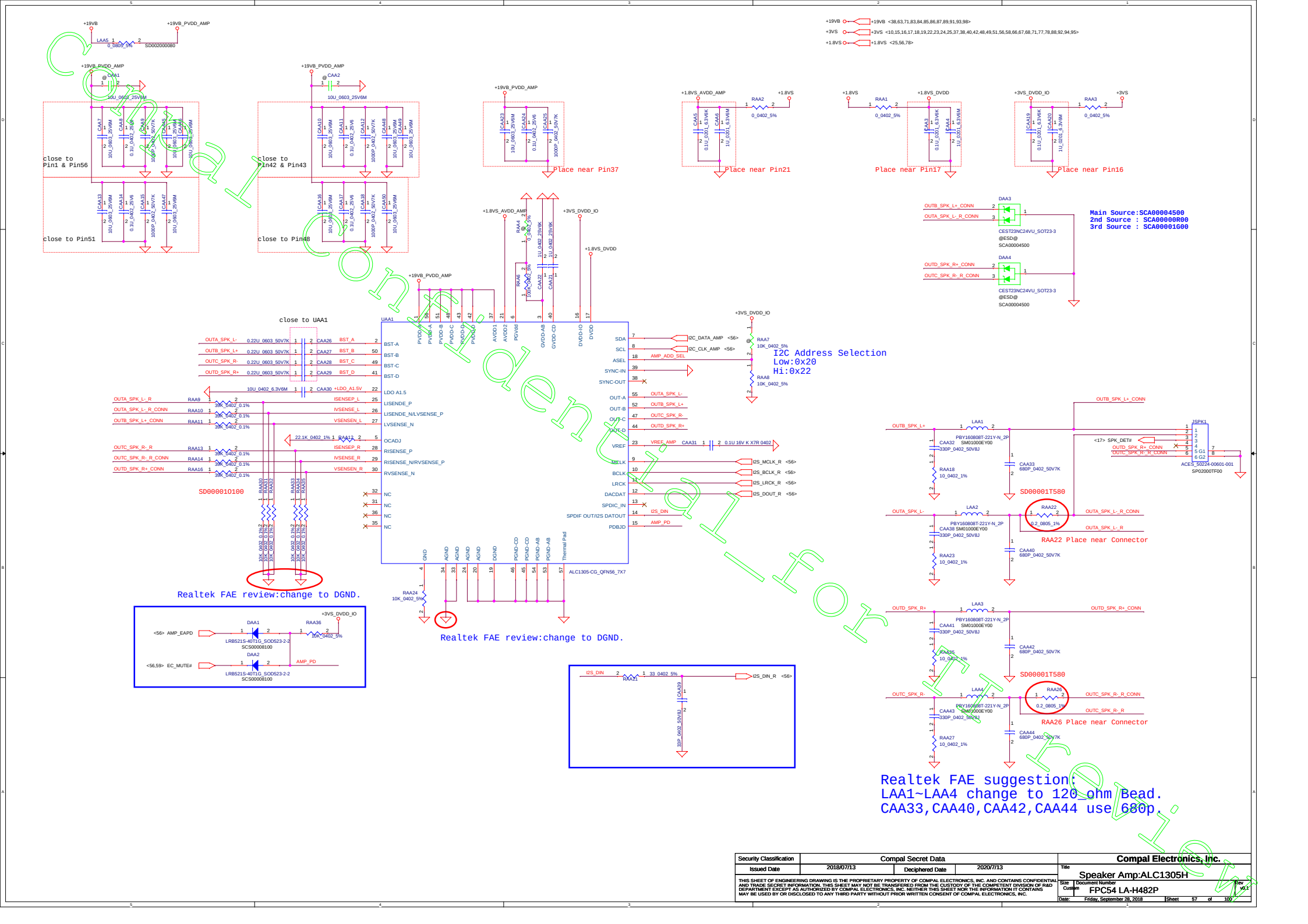

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EC Board ID (DIS, phase) control table

2018 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N17E-G1	33K	43K	56K	75K
R17M-G1-70	100K	130K	160K	200K

2019 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K [0x01]	15K [0x02]	20K [0x03]	27K [0x04]
N18P-G0/G1	33K [0x05]	43K [0x06]	56K [0x07]	75K [0x08]
N18E-G1	100K [0x09]	130K [0x0A]	160K [0x0B]	200K [0x0C]
R19M-G50-70	240K [0x0D]	270K [0x0E]	330K [0x0F]	430K [0x10]

CH0: 85_DATA1: 0x0

2019 OMEN

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K [0x01]	15K [0x02]	20K [0x03]	27K [0x04]
N18P-G0/G1	33K [0x05]	43K [0x06]	56K [0x07]	75K [0x08]
N18E-G1/G2/G3	100K [0x09]	130K [0x0A]	160K [0x0B]	200K [0x0C]

RH264&CH105 Need use after checking

PIR1.48

For Solve tPCH04(Min 9ms) Sequence Timing

PIR1.48

Need Check

PIR2.31

replace to common part 0108

PIR2.31

replace to common part 0108

PIR1.29
PIR2.3
PIR4.3

PIR2.31

PIR2.31

PIR1.38

PIR2.31

CC144/ RC369 place near EC Side

EMI request

Need Check

20mil

Connect to PWR side

KB9022QD LQFP 128P
KB9022@ SA000075S30
S IC KB9022QD LQFP 128P EC CONTROLLER

SA0000BEZ00
KB9022:128KB
KB904x:128KB
KB954x:160KB

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Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 58 of 100

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+3VALW_EC
+5VS

+3VALW_EC <25,58,82>
+5VS <37,38,39,40,56,63,67,78,96>

OMEN New ESB CLK&DAT for Extend I/O

Some EC GPIO maybe change to extend IO control:TBD

+3VALW_EC — RK2012 — 330K_0402_5% — EC_RST#_KC3810

CK201 — 0.1U_0402_16V7K

UK2

<58> KC3810_ESB_CLK — KC3810_ESB_CLK — 1 ESB_CLK
<58> NMI_DBG# — NMI_DBG# — RK209 — NMI_DBG#_KC3810 — 2 GPIO00
KB9542@ 0_0402_5%
*NMI_DBG#: is a debug pin for EC to inform BIOS after press hot key.
EC_RST#_KC3810 — 3 RST#
<58> KC3810_ESB_DAT — KC3810_ESB_DAT — 4 ESB_DAT
*GP:15_Milos_OMENX_HP1X_RFQ_ODM_180518
TP OFF LED on F11 key
12V_EN_KC3810_GPIO01 — 5 GPIO01
<63> TP_LED_OFF# — TP_LED_OFF# — 6 GPIO02
<50> EC_TBT_RESET — EC_TBT_RESET — 7 GPIO03
<25> GPU_ALERT — GPU_ALERT — 8 GPIO04
<73> USB_ON# — USB_ON# — 9 GPIO05
<63> KB_GPO1# — 10 GPIO06
<63> KB_GPO2# — 11 GPIO07/CAS_CLK
12 GND

13 TEST_EN#
14 GPIO08/CAS_DAT
15 GPIO09 — USB_CTL1 — USB_CTL1 <71>
16 GPIO0A — USB_CTL2 — USB_CTL2 <71>
17 GPIO0B — USB_CTL3 — USB_CTL3 <71>
18 GPIO0C/PWM0 — USB_CHARGE_EN — USB_CHARGE_EN <71>
19 GPIO0D/PWM1 — GPU_OVERT# — GPU_OVERT# <25>
20 GPIO0E/PWM2 — LAN_PWR_EN — LAN_PWR_EN <51>
21 GPIO0F/PWM3 — WL_PWREN_EC# — WL_PWREN_EC# <52>
22 GPIO10/ESB_RUN# — EC_MUTE# — EC_MUTE# <56,57>
23 GPIO11/BaseAddOpt
24 VCC — +3VALW_EC
25 GND

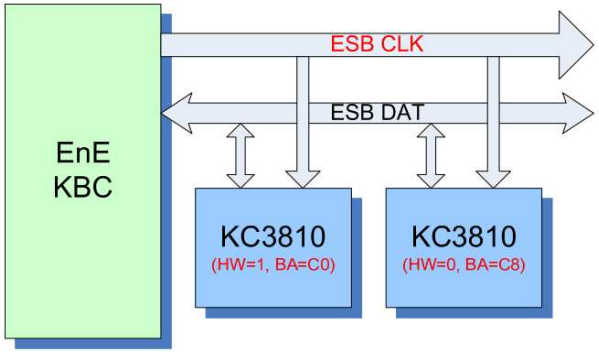
KC3810NF-A0_QFN24_4X4
SA00002AI00

CK202 — 0.1U_0201_10V6K

USB_CTL3 — RK28 — 100K_0402_5%

以下14根Pin 建議可以接到external I/O 3810,
1. USB_CTL1(GPIO4B Pin84),
2. USB_CTL2(GPIO3F Pin72),
3. USB_CTL3(GPIO1D Pin38),
4. USB_CHARGE_EN(GPIO1A Pin36),
5. GPU_OVERT#(GPIO0D Pin19) => DPF50 NO USE
6. LAN_PWR_EN(GPIO4D Pin86),
7. WL_PWREN_EC#(GPIO61 Pin98),
8. DCHG_I(GPIO40 Pin73) => DPF50 NO USE
9. USB_ONI#(GPIO37 Pin 121),
10. LED : 5 Pin.

Some EC GPIO maybe change to extend IO control:TBD



+5VS
RK210 — 0_0402_5%
<97> 12V_EN — RK211 — 0_0402_5% — 12V_EN_KC3810_GPIO01

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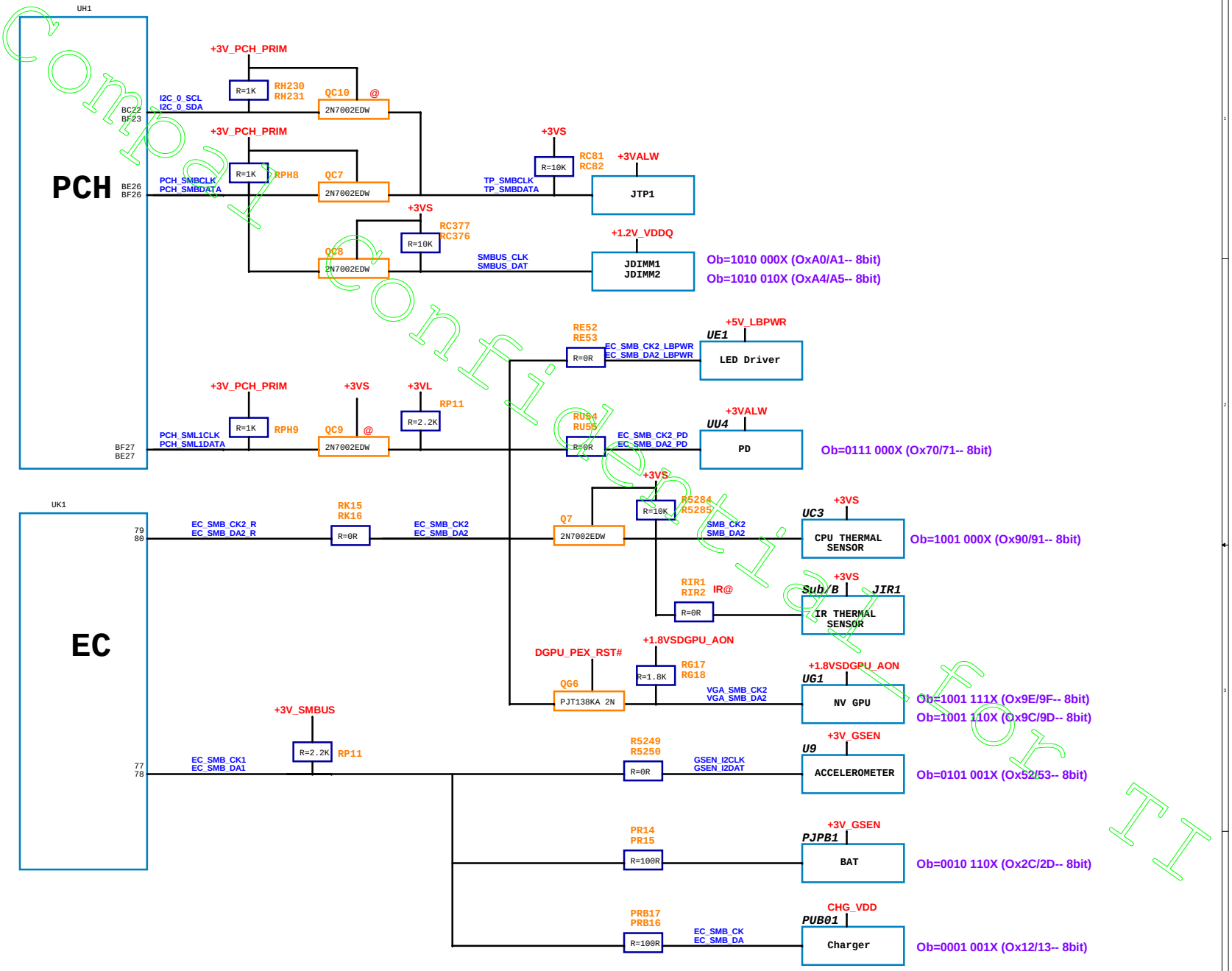

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Title	SMBus Block Diagram
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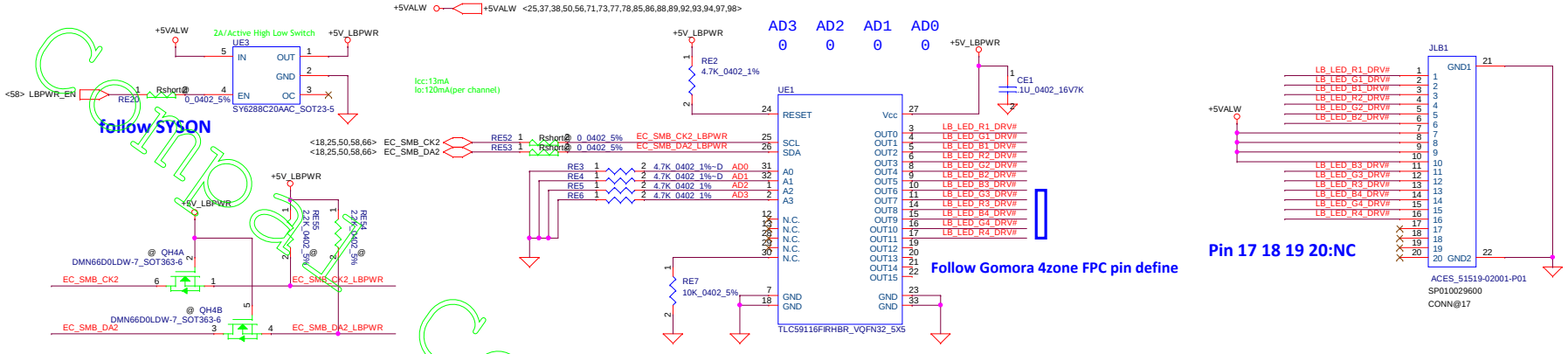

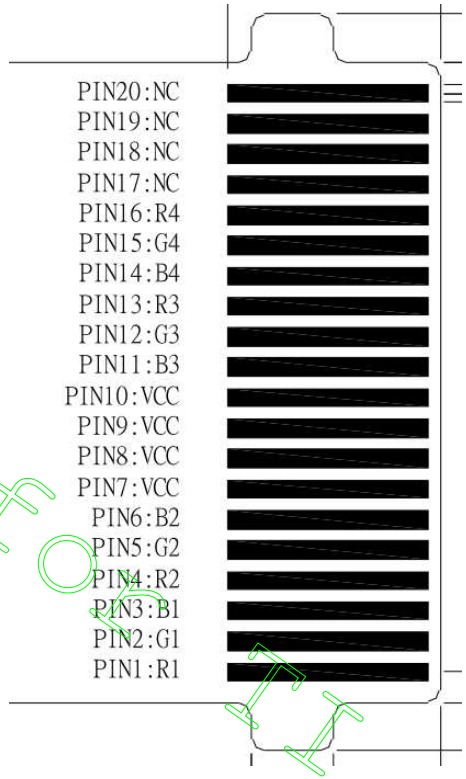

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Compal Electronics, Inc.			
Title	A Cover BKL		
Size	Document Number		Rev
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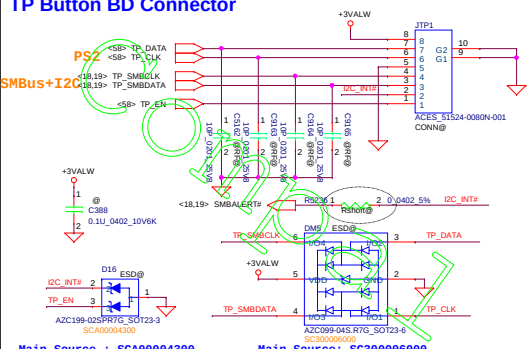
TP Button BD Connector

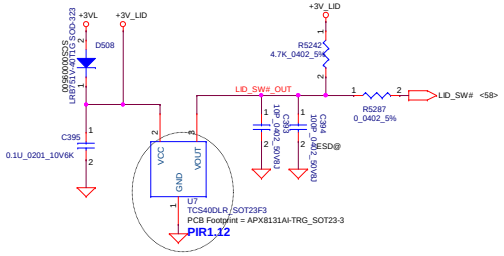


Main Source : SCA00004300
2nd Source : SCA00001T00
3rd Source : SC600001600

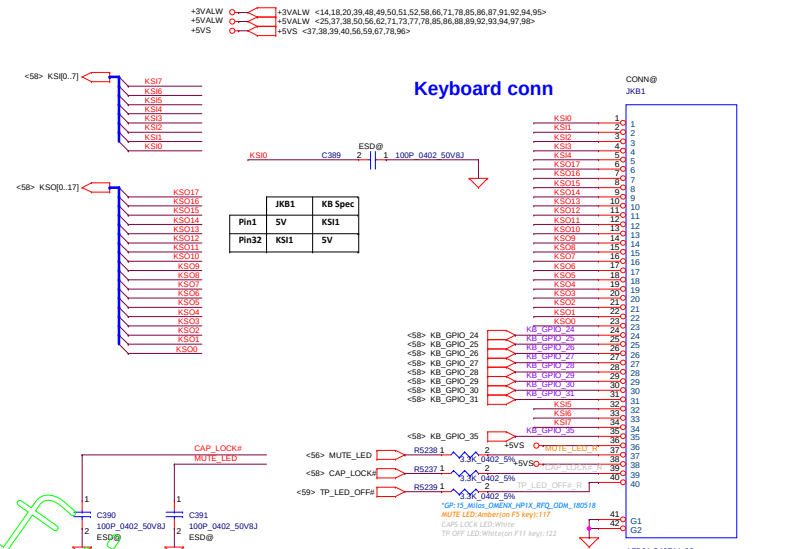
Main Source: SC300006000
2nd Source : SC300001G00
3rd Source : SC300003S00

Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock I_{SINK} or I_{SRA}: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. I_{SINK} or I_{SRA}: 8 mA max.
7	/INT (/ATTN)	O	For SMBus application, low active, indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP

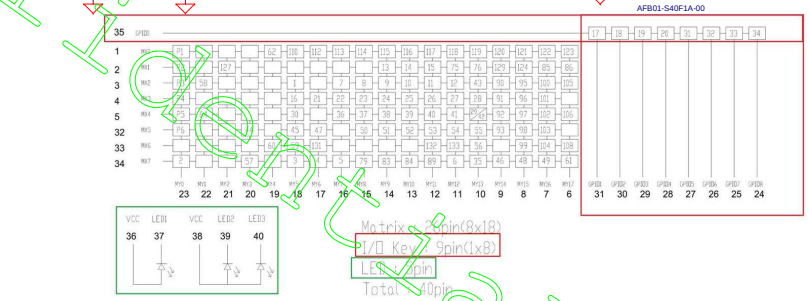
Lid Switch (Hall Effect Sensor)

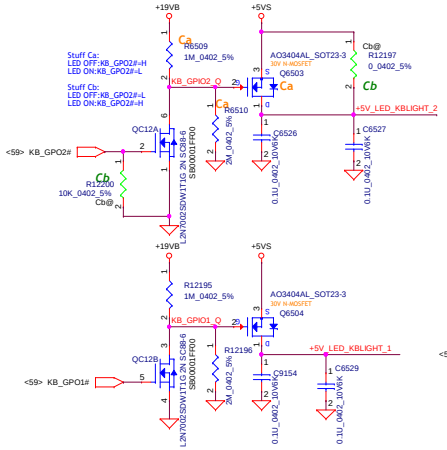


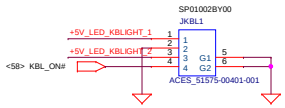
Keyboard conn



JKB1	KB Spec
Pin1	5V
Pin32	KSI1
	5V







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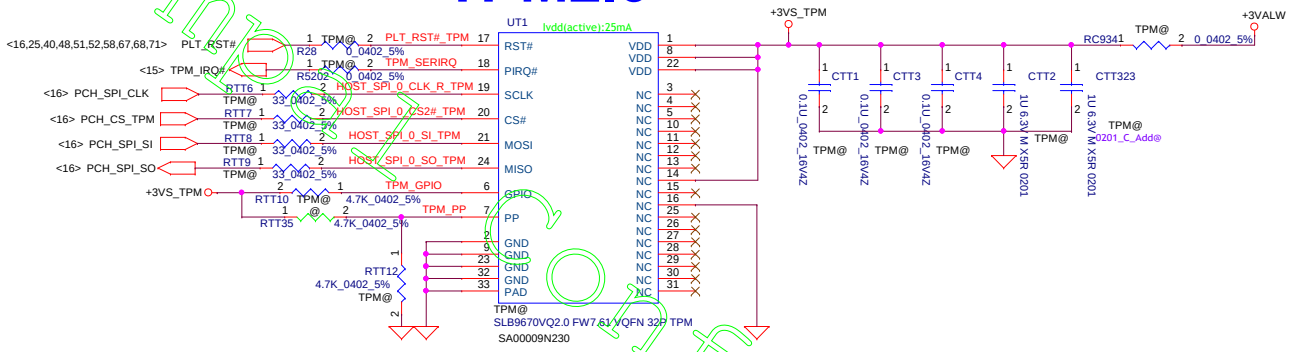
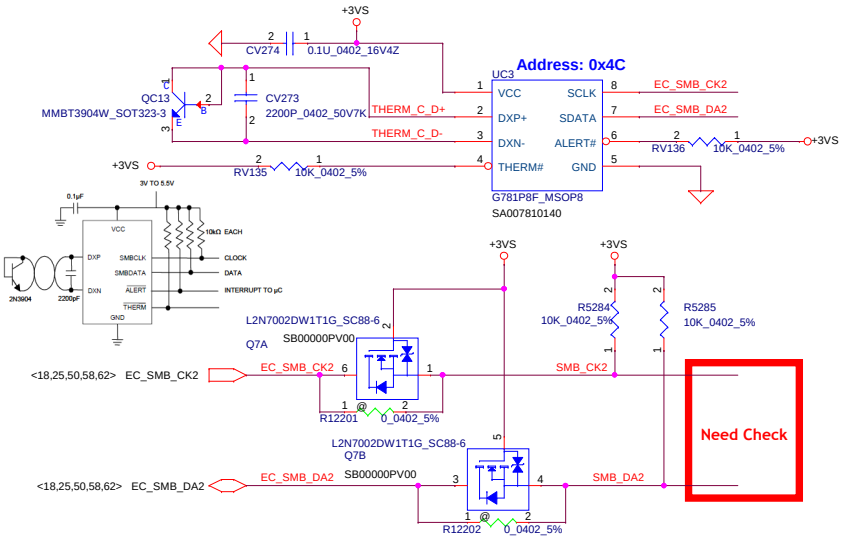
+3VALW <+3VALW <14,18,20,39,48,49,50,51,52,58,63,71,78,85,86,87,91,92,94,95>
+3VS <+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,48,49,51,56,57,58,67,68,71,77,78,88,92,94,95>

TPM2.0



CPU THERMAL SENSOR



ACCELEROMETER
ST Micro HP2DC

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Hmax=1.0mm

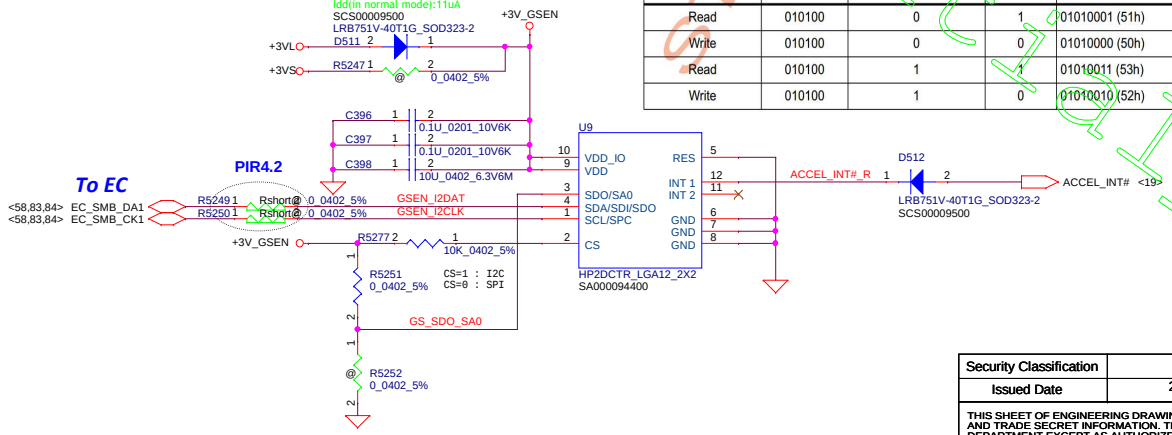
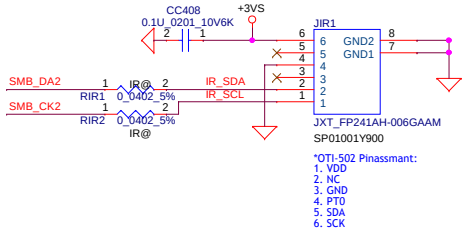


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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Title: TPM&Thermal&G-sensor

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M.2 SSD:1

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		42	N/C		
41	PETn0	PCIe TX		44	N/C		
43	PETp0	PCIe TX		46	N/C		
45	GND	Return current path		48	N/C		
47	PERn0	PCIe Rx		50	PERST#		
49	PERp0	PCIe Rx		52	CLKREQ#		
51	GND	Return current path					

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

2.5" SATA HDD

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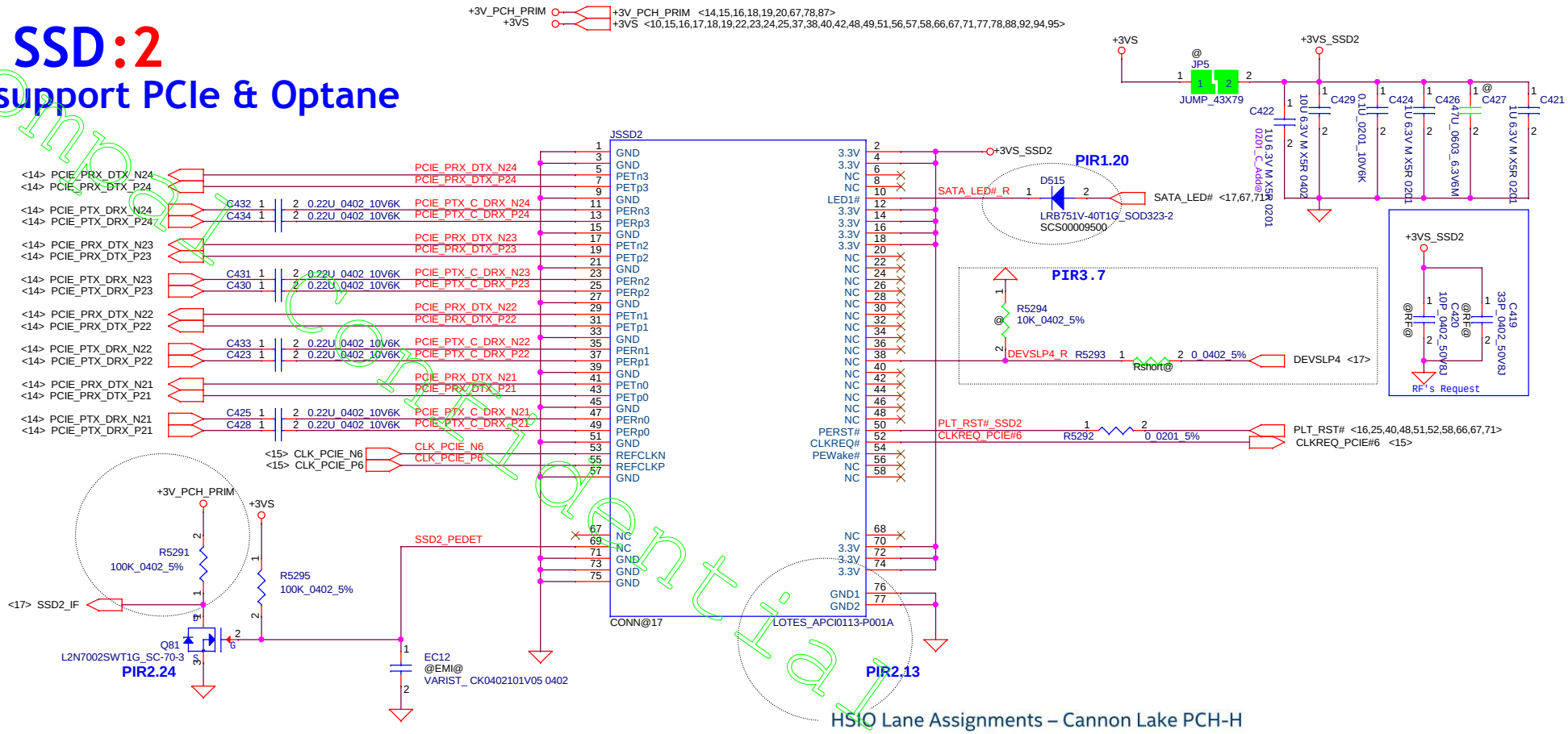
M.2 SSD:2

Only support PCIe & Optane



36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

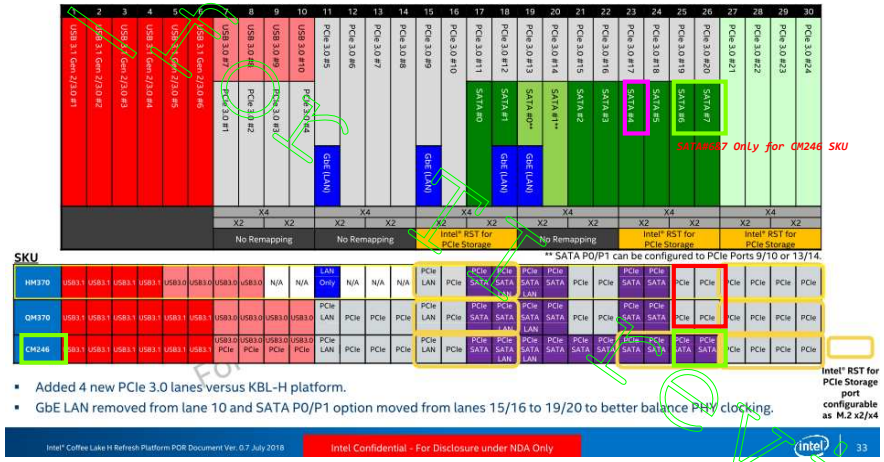
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	Return Current Path	40
41	+B TXP	Transmitter Differential Signal Pair	42
43	-B TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	-A RXN	Receiver Differential Signal Pair	48
49	+A RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

HSIO Lane Assignments – Cannon Lake PCH-H



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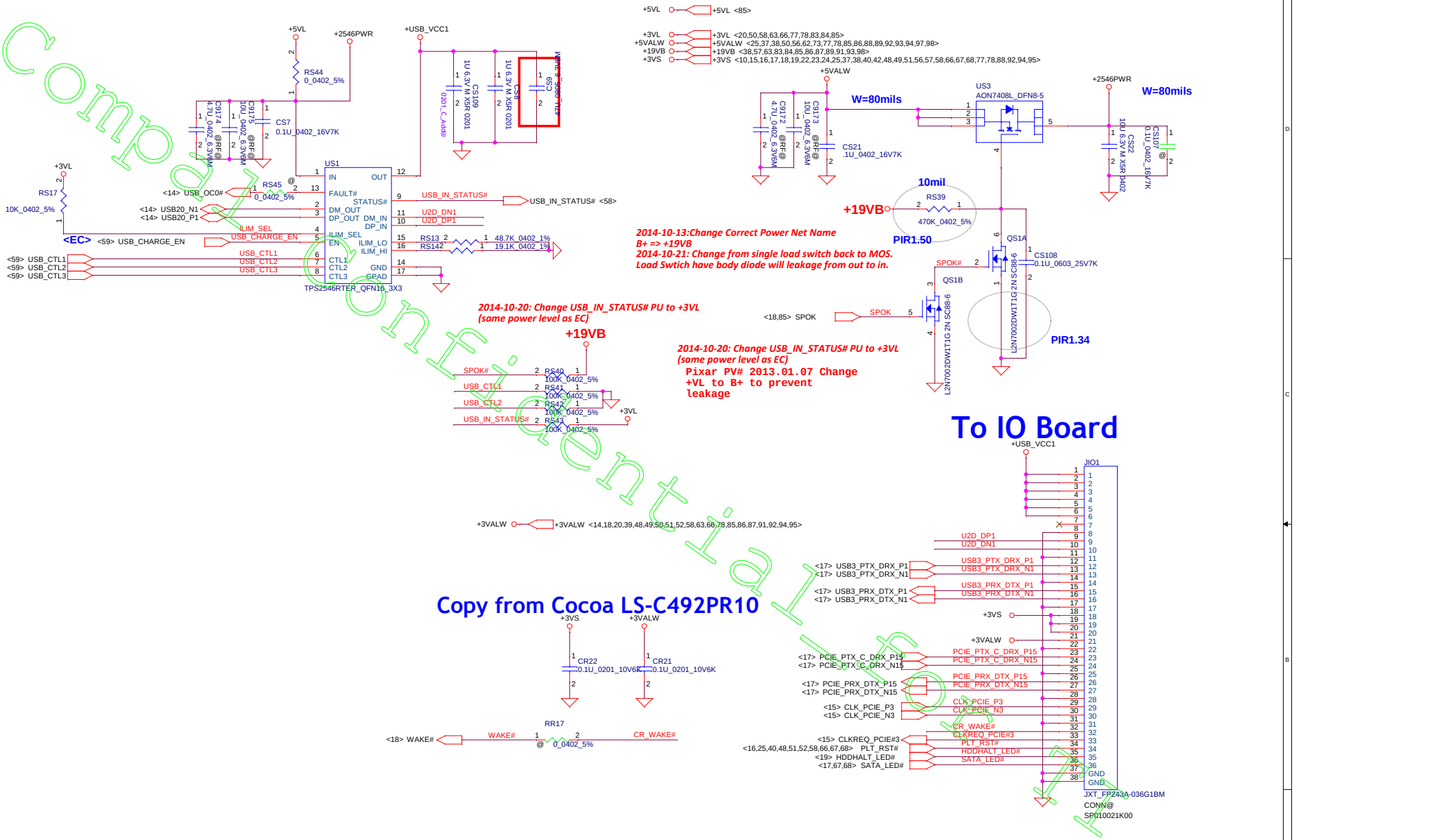

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Title: USB Charger

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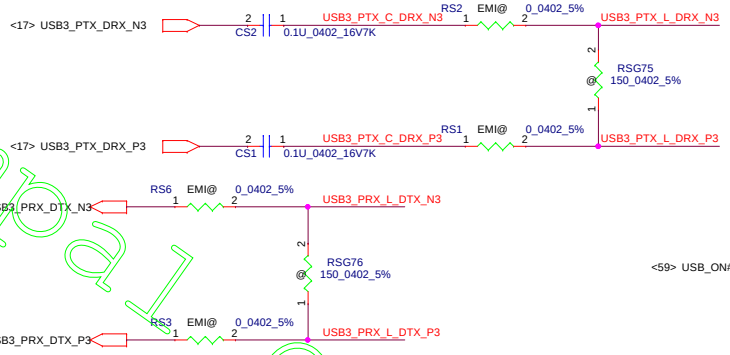
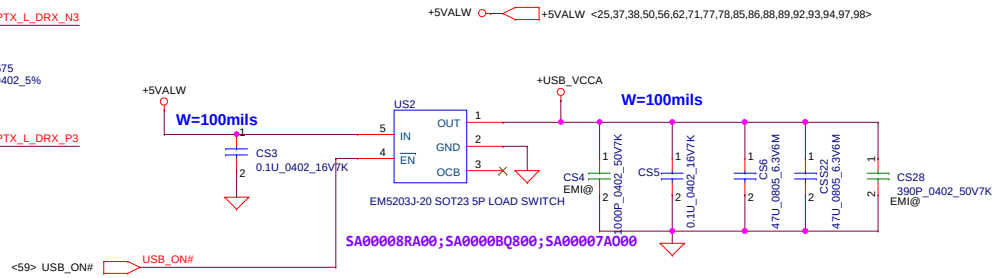
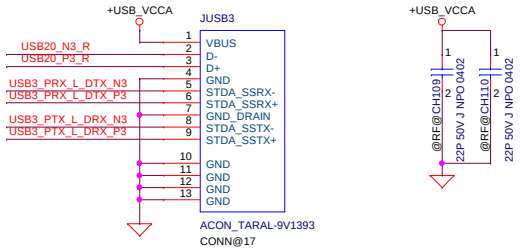
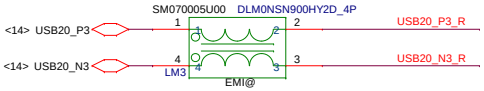




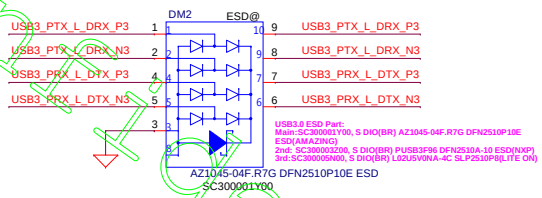
USB2.0/USB3.0 port 1



2018-03-01:
Del reserved EMI part on MV for DFB request
RS47,RS48



USB2.0 Choke Part:
Main:SM070005U00, S COM FI_ MURATA
DLM0NSN900HY2D(MURATA)
2nd: SM070004X00, S COM FI_ PANASONIC
EXC14CE900U(PANASONIC)



USB3.0 ESD Part:
Main:SC300001Y00, S DIO(BR) AZ1045-04F.R7G DFN2510P10E ESD(AMAZING)
2nd: SC300003Z00, S DIO(BR) PUSB3F96 DFN2510A-10 ESD(NXP)
3rd:SC300005N00, S DIO(BR) L02U5V0NA-4C SLP2510P8(LITE ON)

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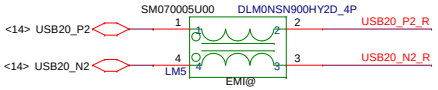
Del reserved EMI part on MV for DFB request
RS49,RS50



USB2.0 Choke Part:
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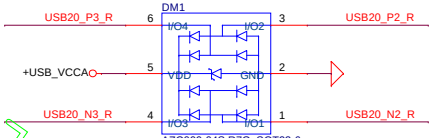
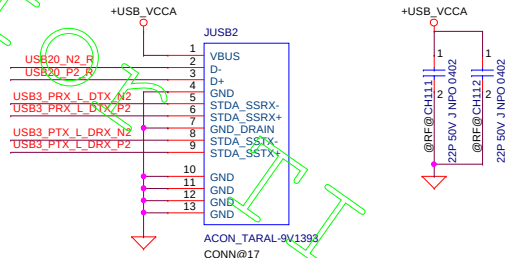
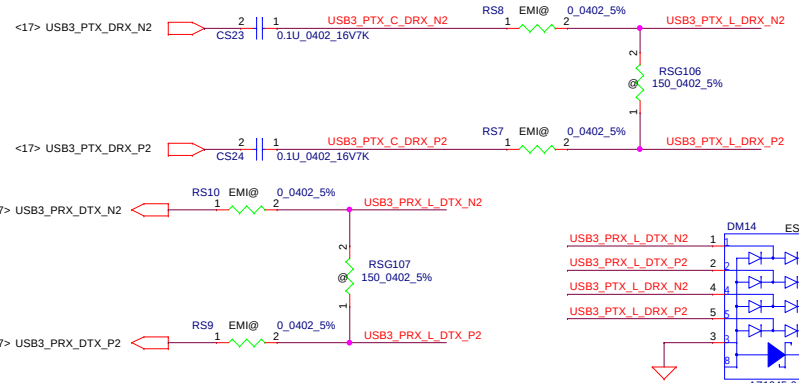
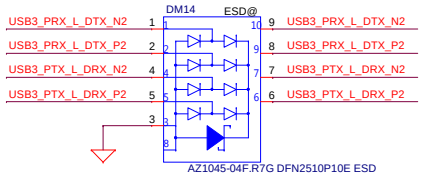


USB2.0/USB3.0 port 2







USB3.0 ESD Part:
Main:SC300001Y00, S DIO(BR) AZ1045-04F.R7G DFN2510P10E ESD(AMAZING)
2nd: SC300003Z00, S DIO(BR) PUSB3F96 DFN2510A-10 ESD(NXP)
3rd:SC300005N00, S DIO(BR) L02U5V0NA-4C SLP2510P8(LITE ON)

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Title: USB 3.0/2.0 conn

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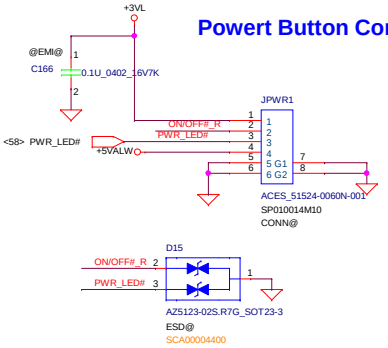
Powert Button Connector



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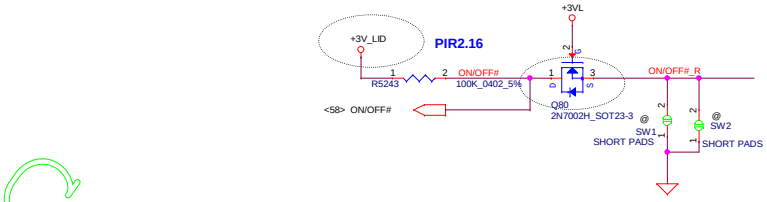
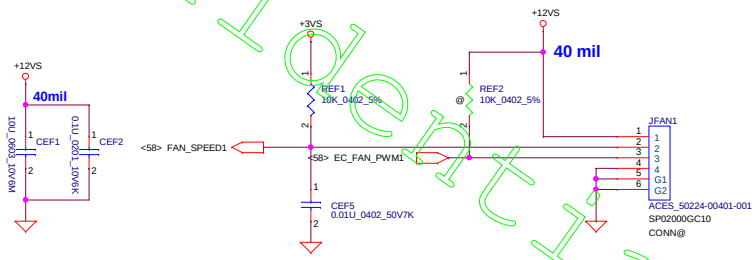
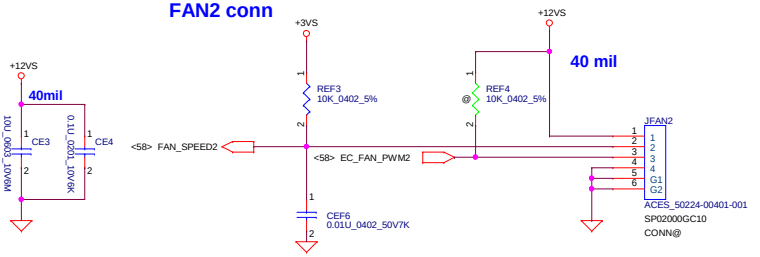


FAN1 conn



FAN2 conn



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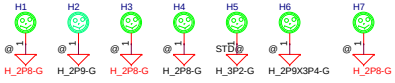
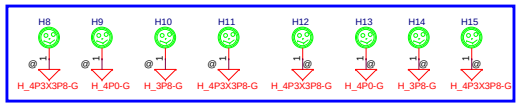
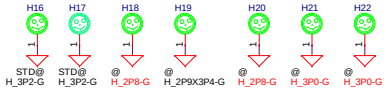


CPU/GPU bracket





Fiducial Mark

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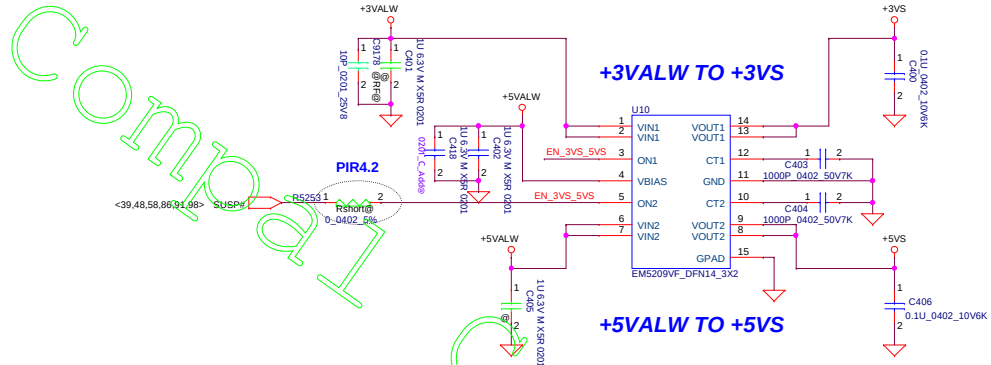

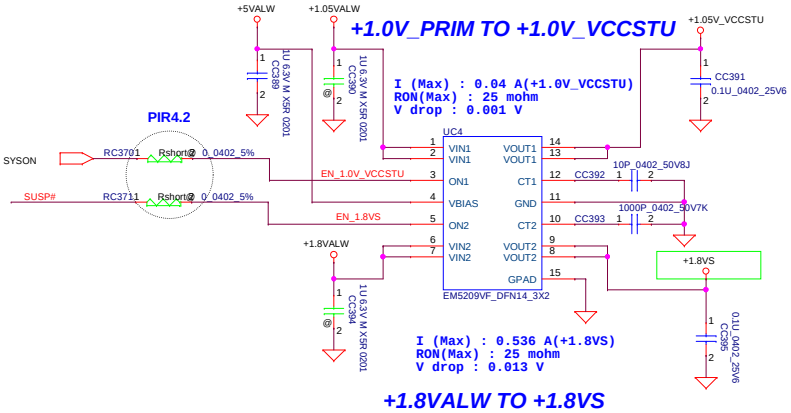

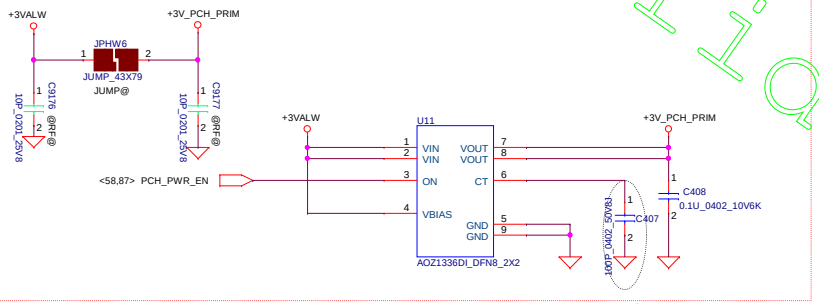

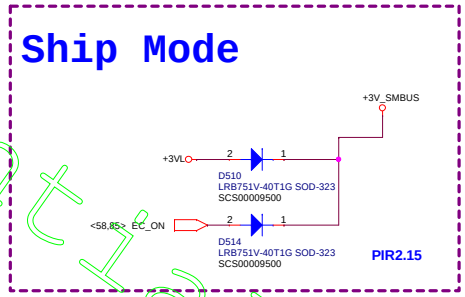

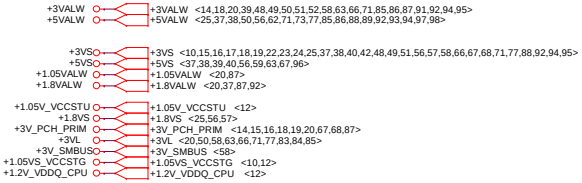

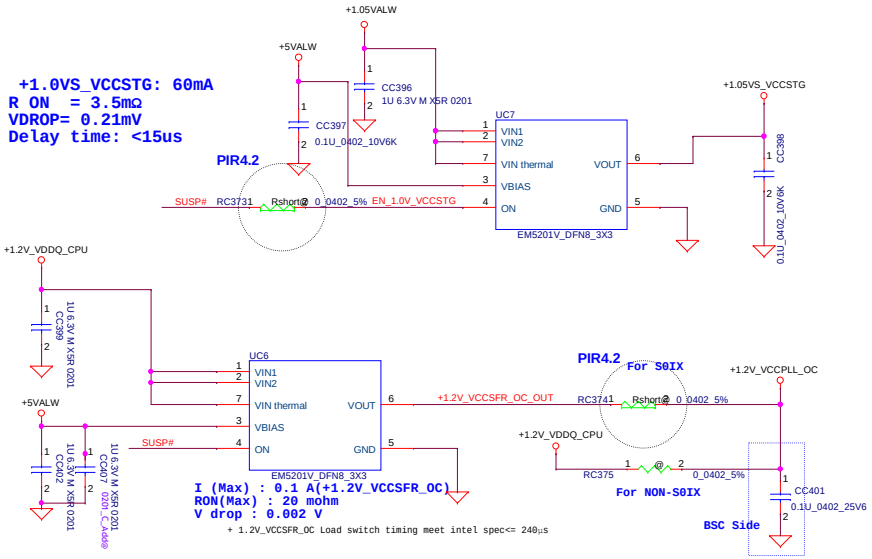

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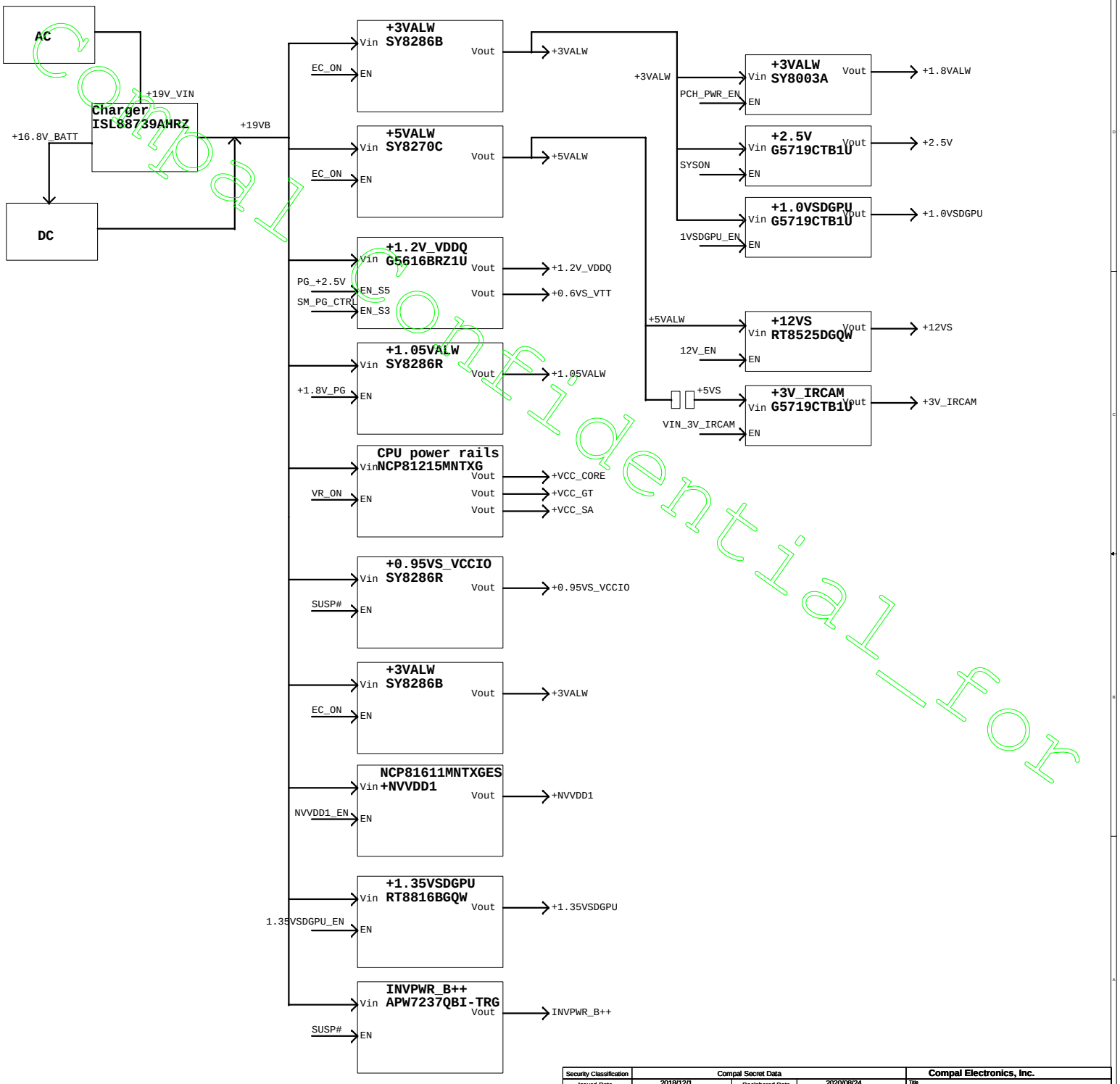

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Title	Power Block Diagram		
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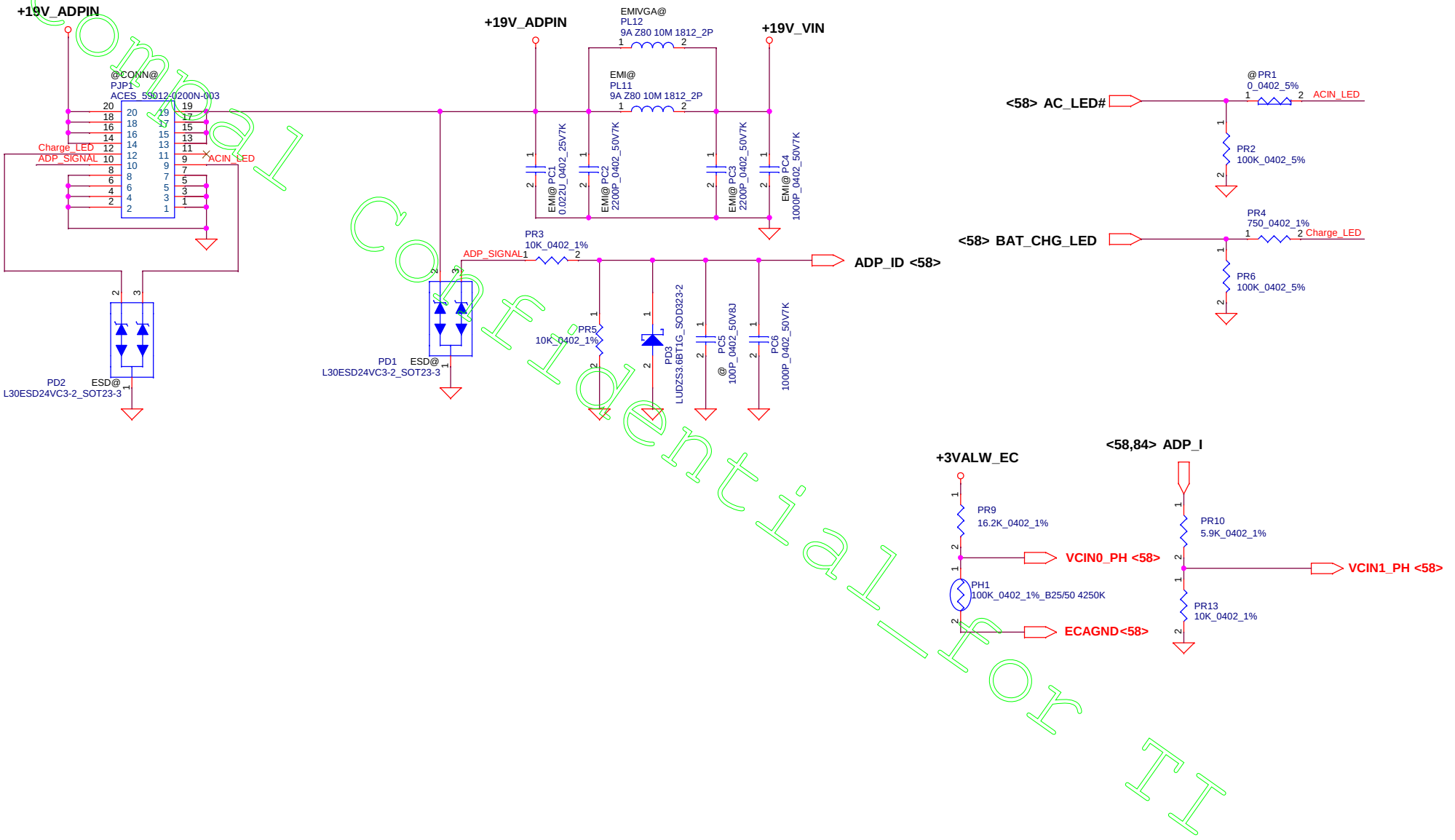

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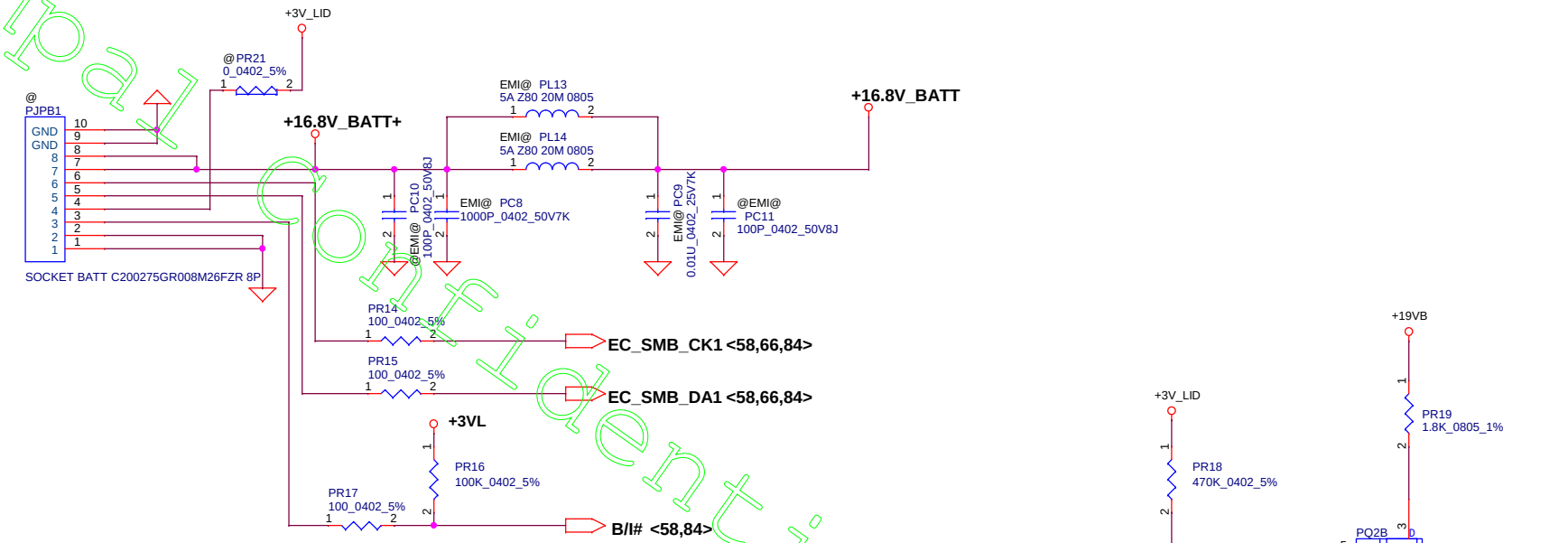

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Title: BATT Conn

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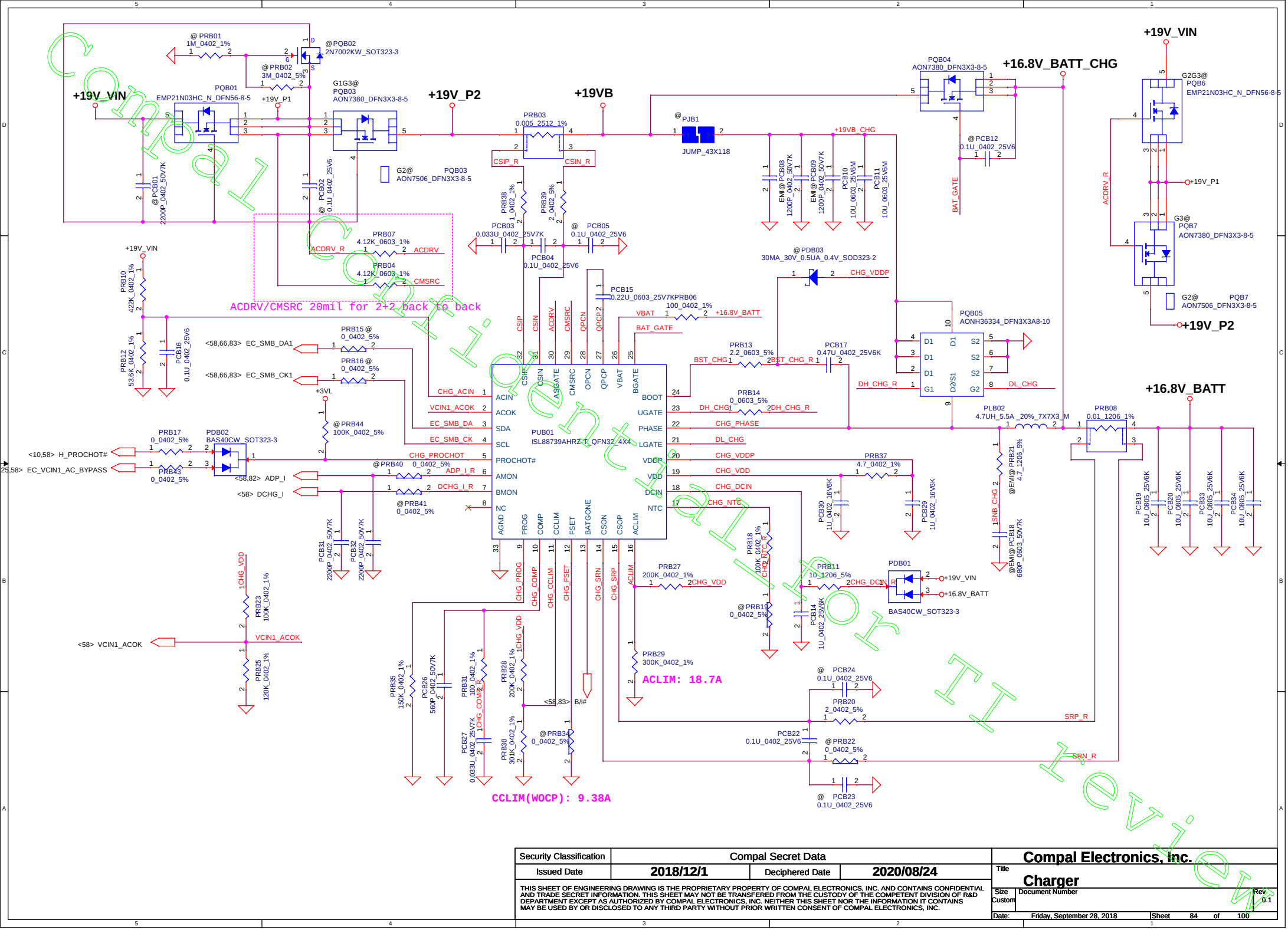
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ACDRV/CMSRC 20mil for 2+2 pack to back
ACLIM: 18.7A
CCLIM(WOCP): 9.38A
PUB01 ISL88739AHRZ-T QFN32_4X4
PQB01 EMP21N03HC_N_DFN56-8-5
PQB02 2N7002KW_SOT323-3
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PDB03 30MA_30V_0.5UA_0.4V_SOD323-2
PJB1 JUMP_43X118
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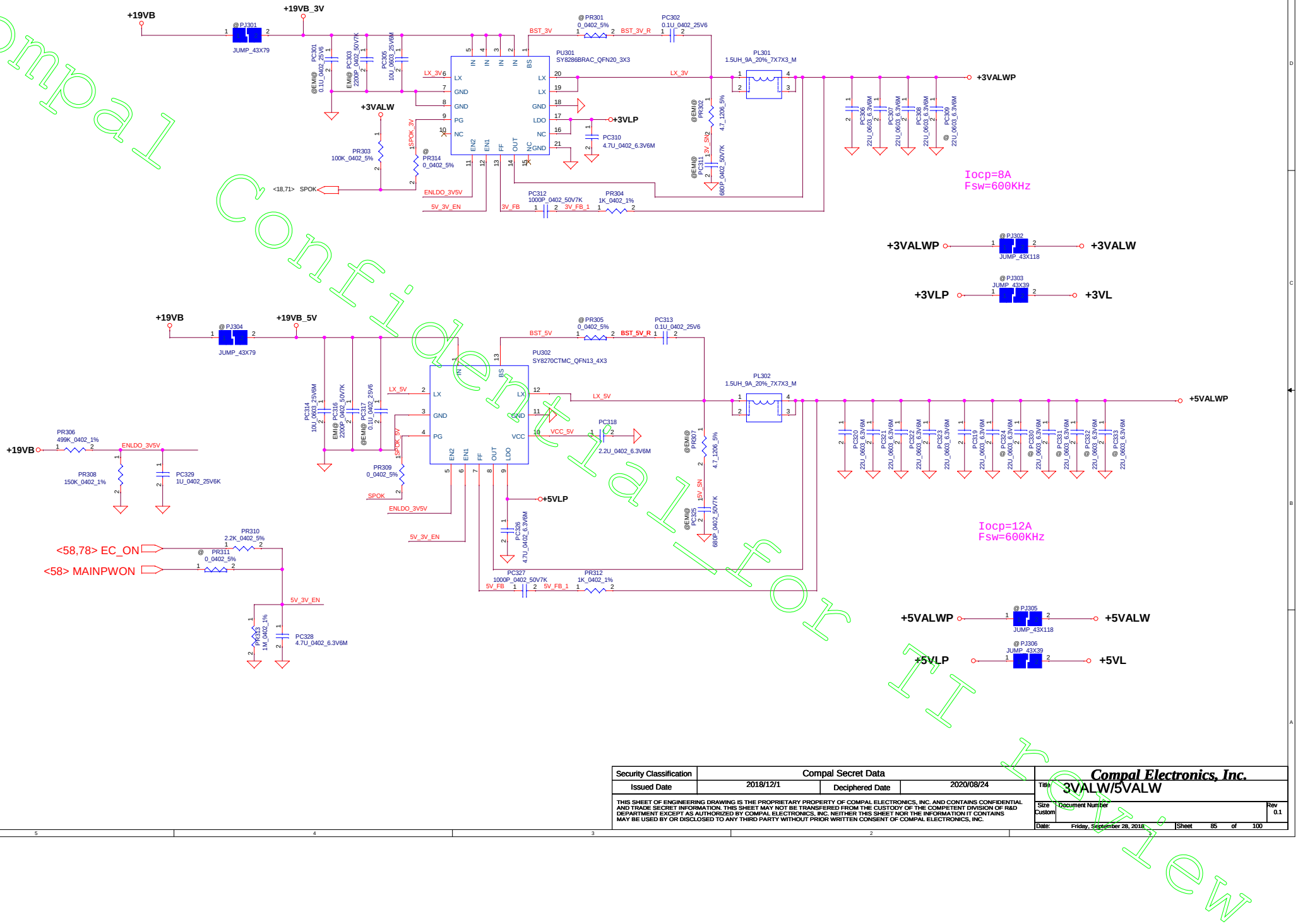

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Title: 3VALW/5VALW

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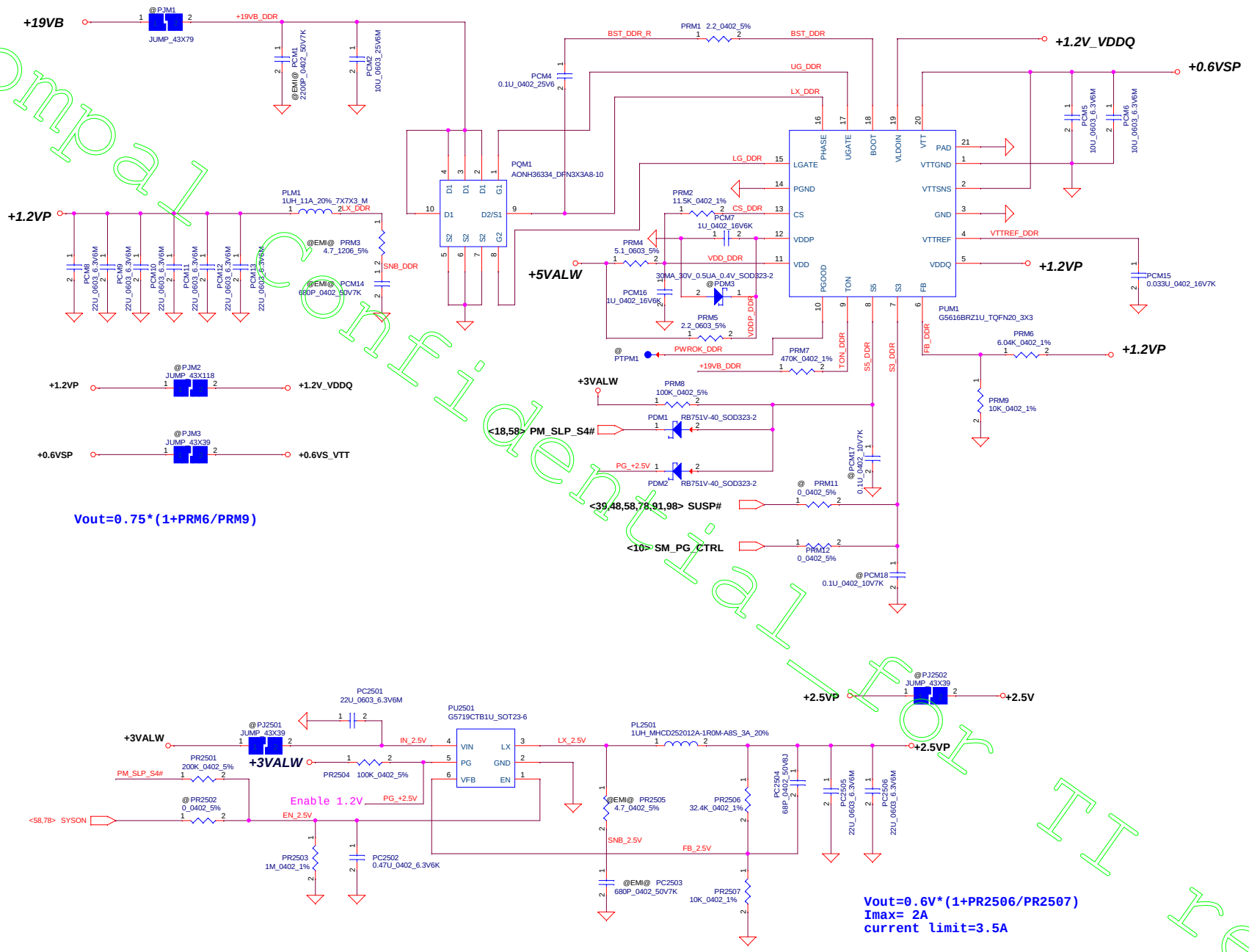

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Title: 1.2VP/0.6VSP/2.5V

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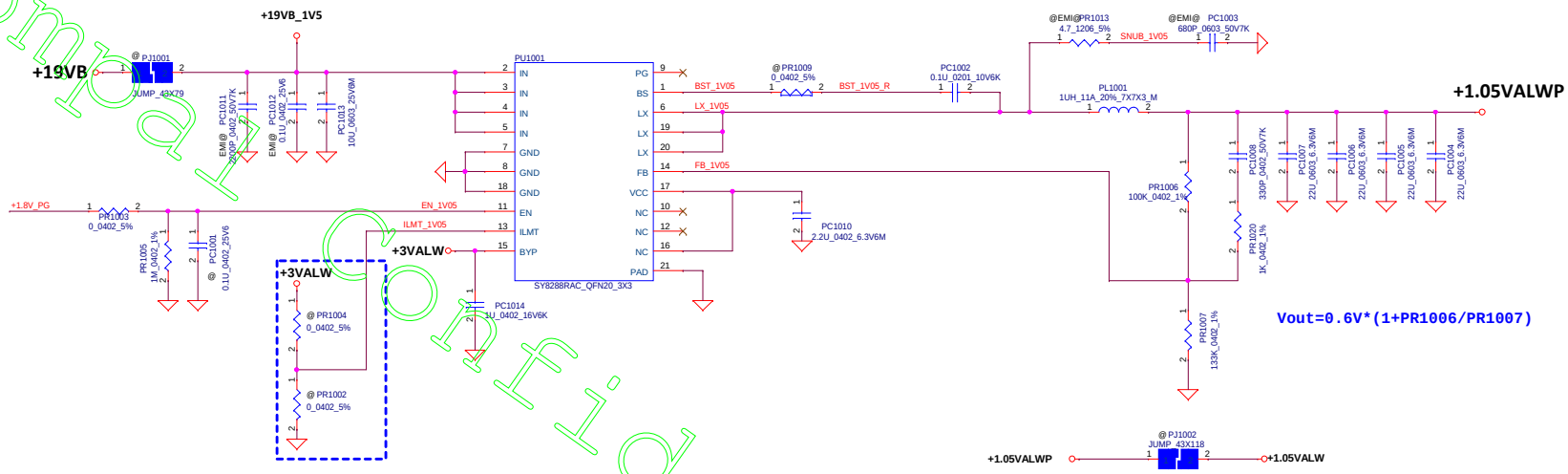

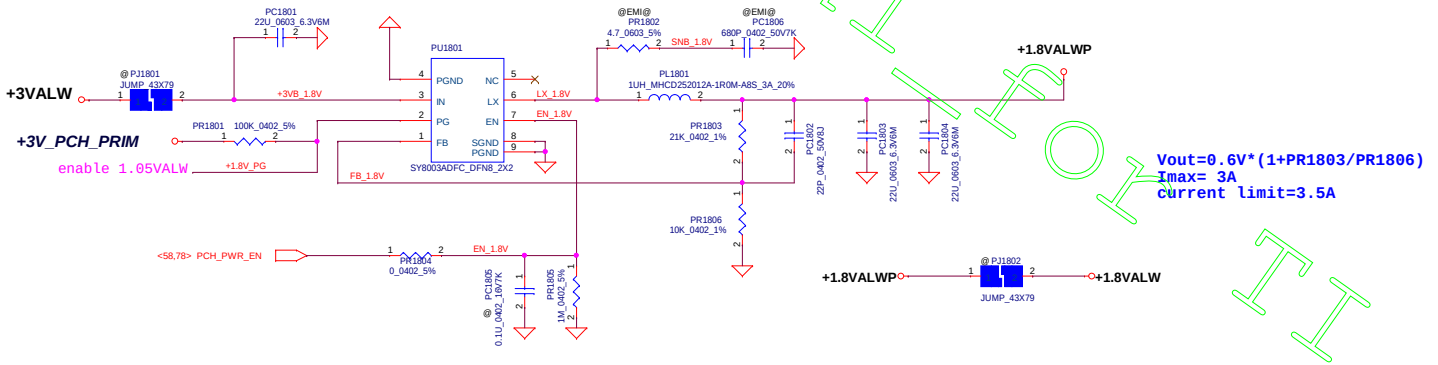

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Title: 1.05V/1.8V

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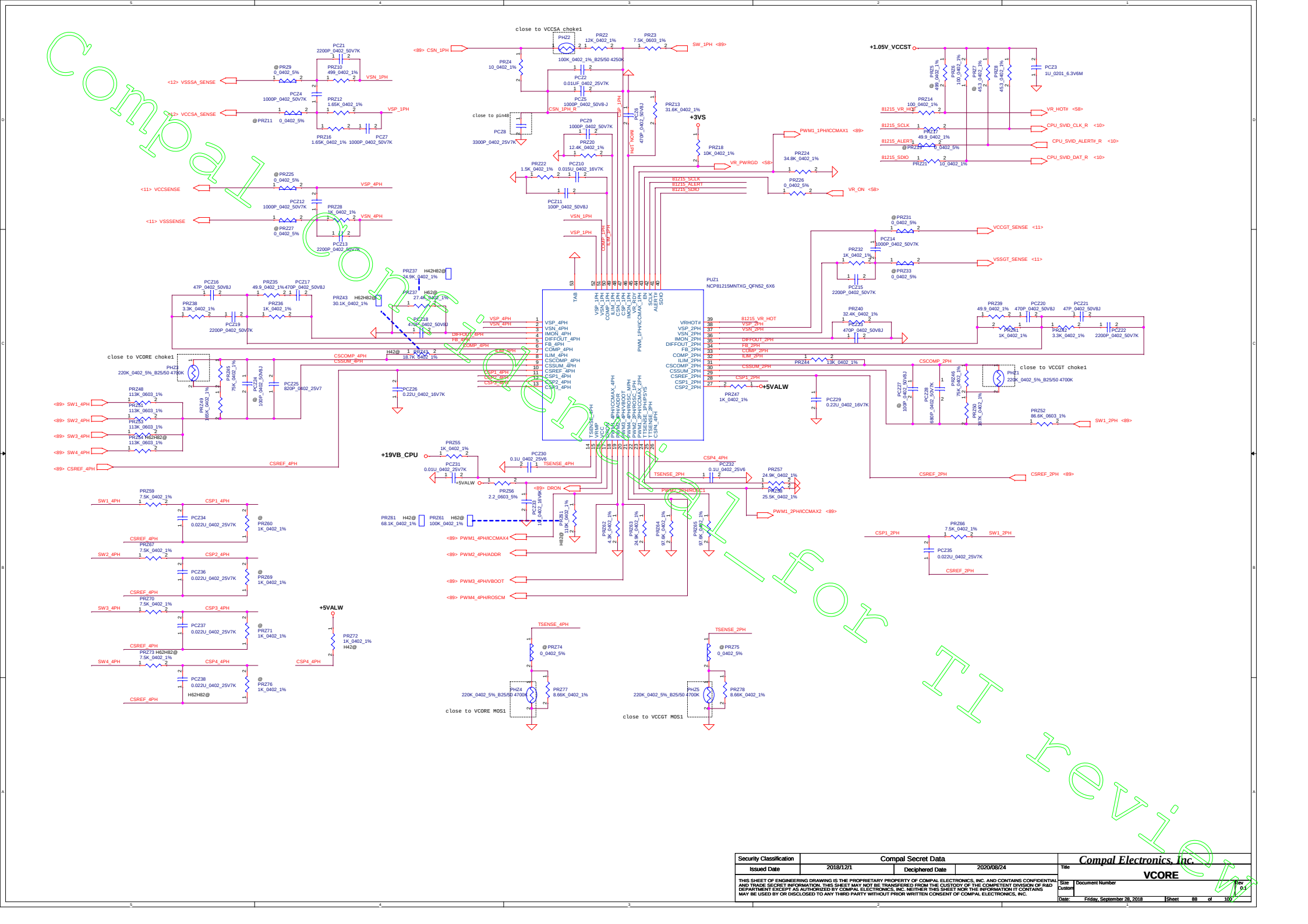
Date: Friday, September 28, 2018 | Sheet 87 of 100



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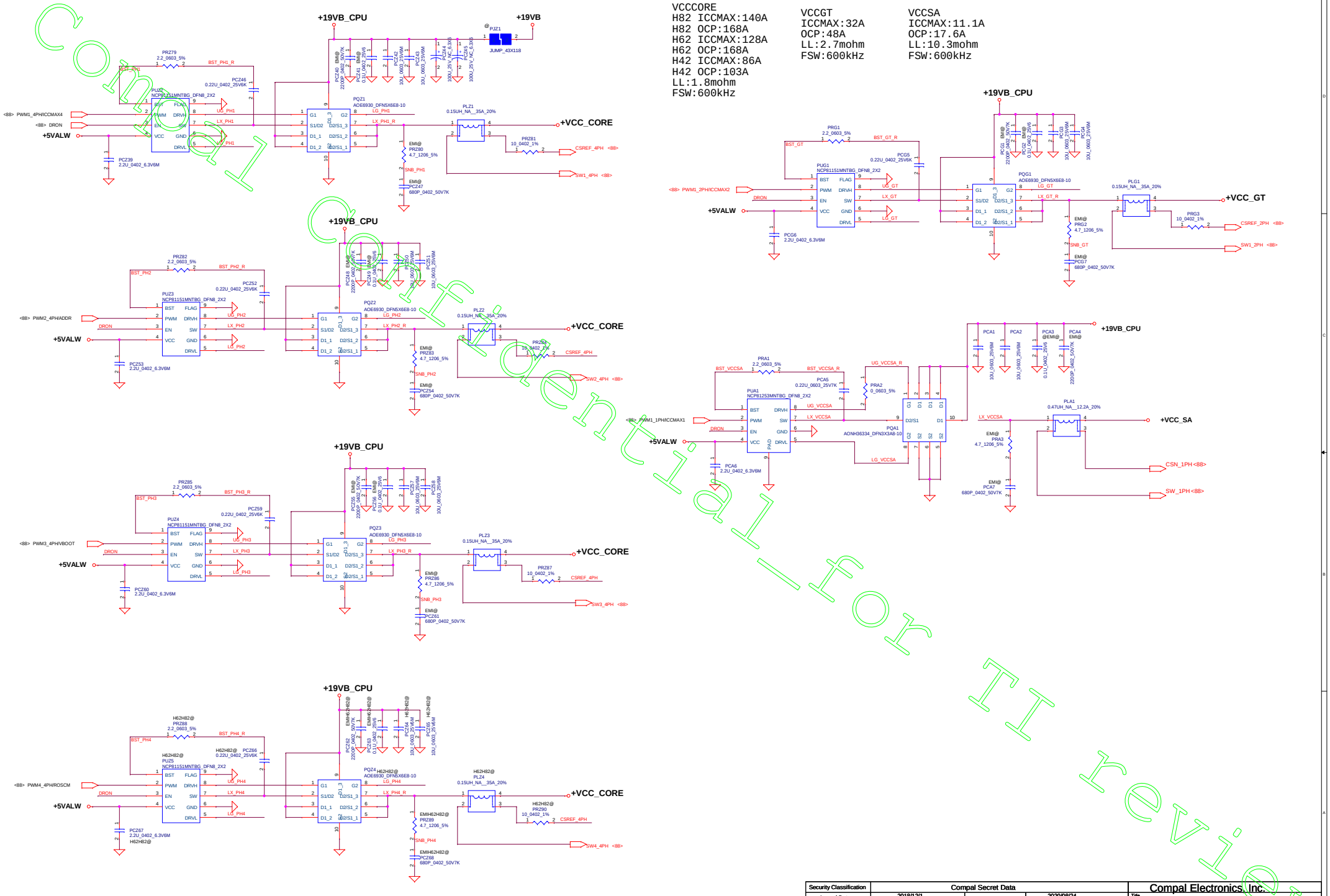
Compal Electronics, Inc.	
Title	VCORE
Size: Custom	Document Number:
Rev: 0.1	
Date: Friday, September 28, 2018	Sheet 88 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/1	Deciphered Date 2020/08/24	Title: VCORE SW
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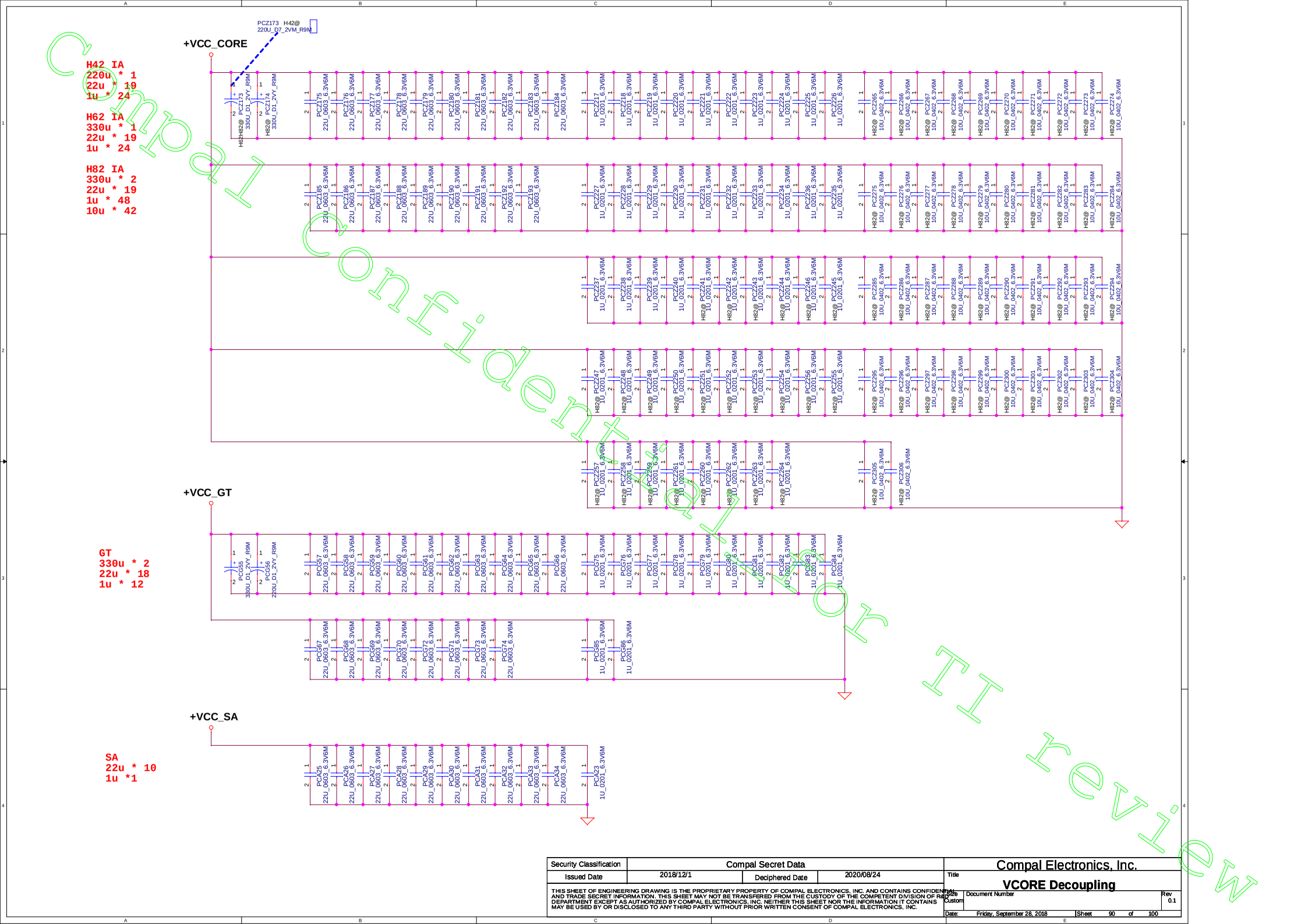
			Date: Friday, September 28, 2018; Sheet 89 of 100



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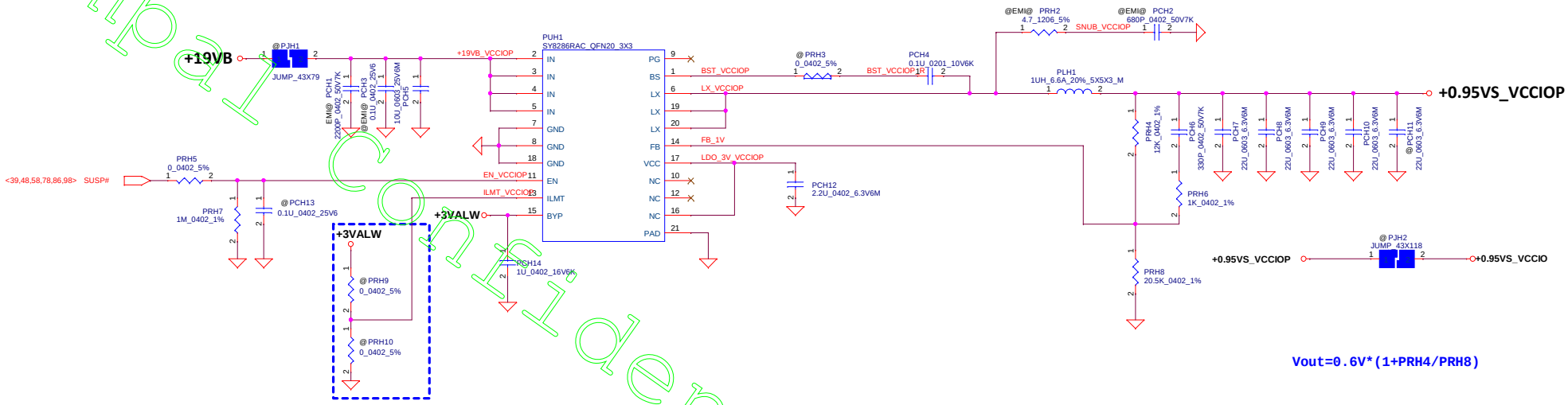
Compal Electronics, Inc.

Title: VCORE Decoupling

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 90 of 100



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Issued Date	2018/12/1	Deciphered Date	2020/08/24

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Title: **VCCIO**

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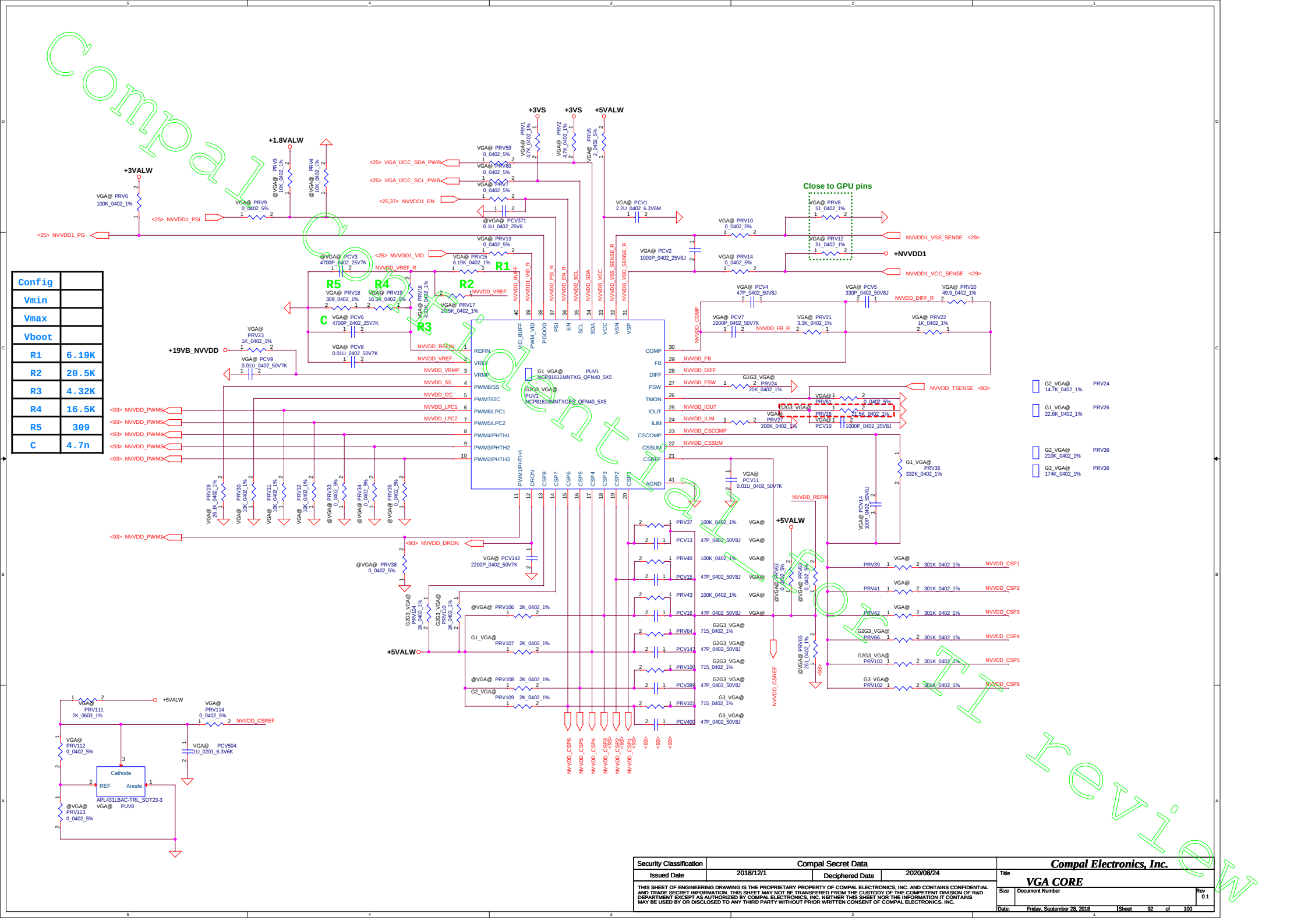
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Close to GPU pins
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+1.8VALW
+3VALW
+19VB_NVVDD
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NVVDD_TSENSE
NVVDD_CSREF
NVVDD_REFIN
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NVVDD_BUFF
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NVVDD_CSP6
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R4
R5
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Vmax
Vboot
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R2 20.5K
R3 4.32K
R4 16.5K
R5 309
C 4.7n
REFIN
VREF
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PWM8/SS
PWM7/I2C
PWM6/LPC1
PWM5/LPC2
PWM4/PHTH1
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FB
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FSW
TMON
IOUT
ILIM
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Compal Electronics, Inc.
VGA CORE
Friday, September 28, 2018
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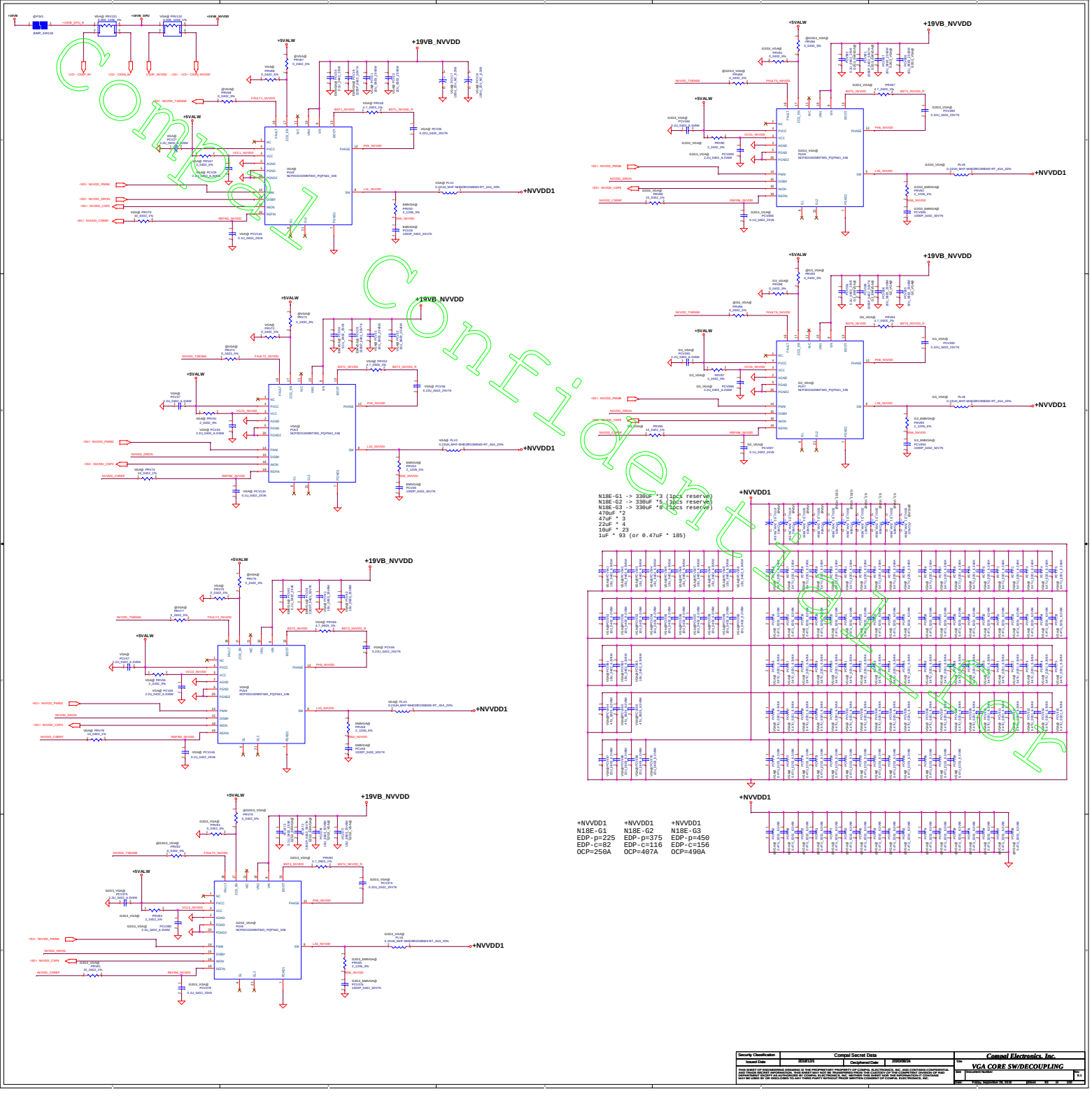

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Issued Date	2018/12/5	Deciphered Date	2020/08/04
			Title: VGA CORE SW/DECOUPLING
			Size: Document Number: Rev: 0.4
			Date: Friday, September 04, 2020 Sheet: 63 of 100

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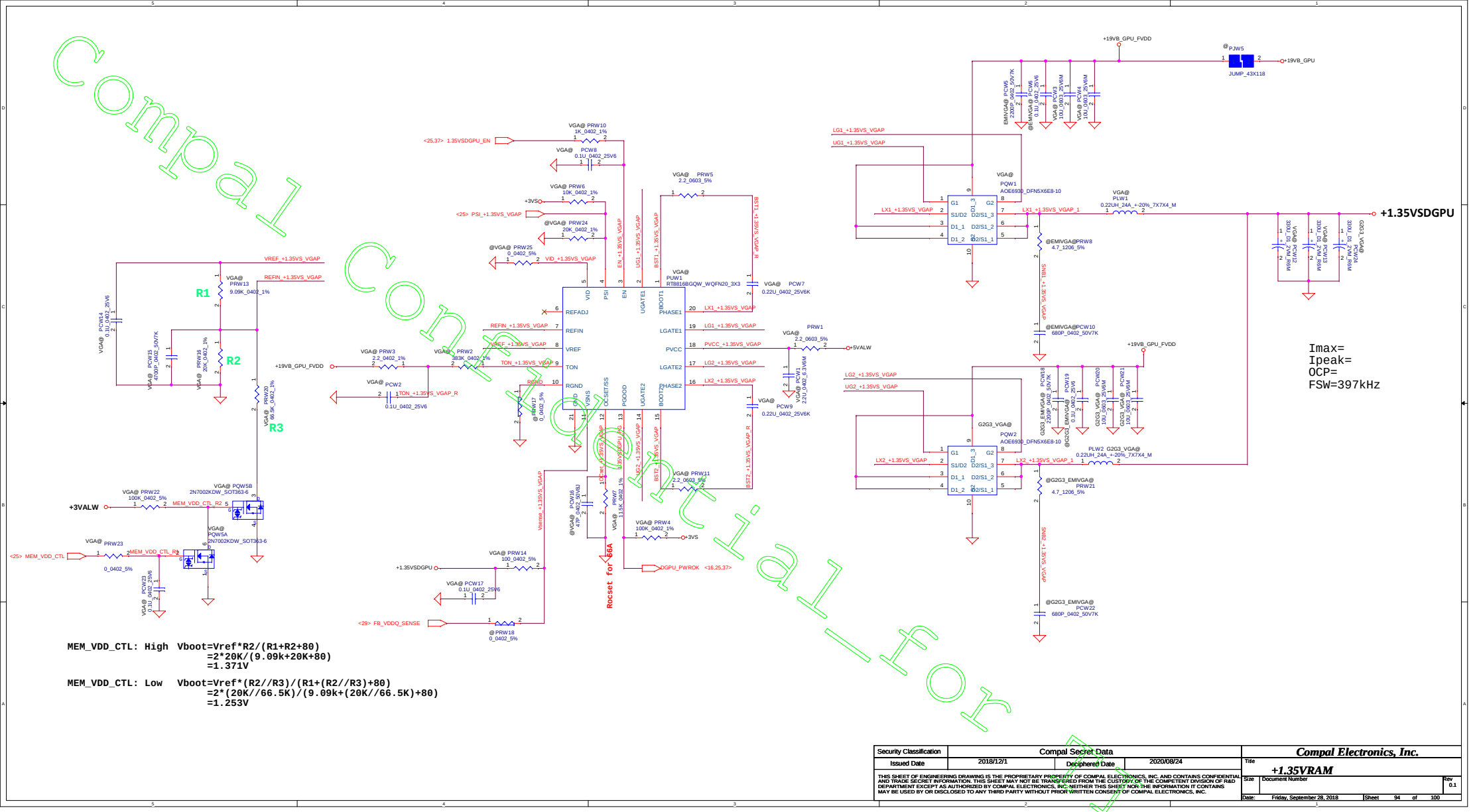

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Title: **+1.35VRAM**

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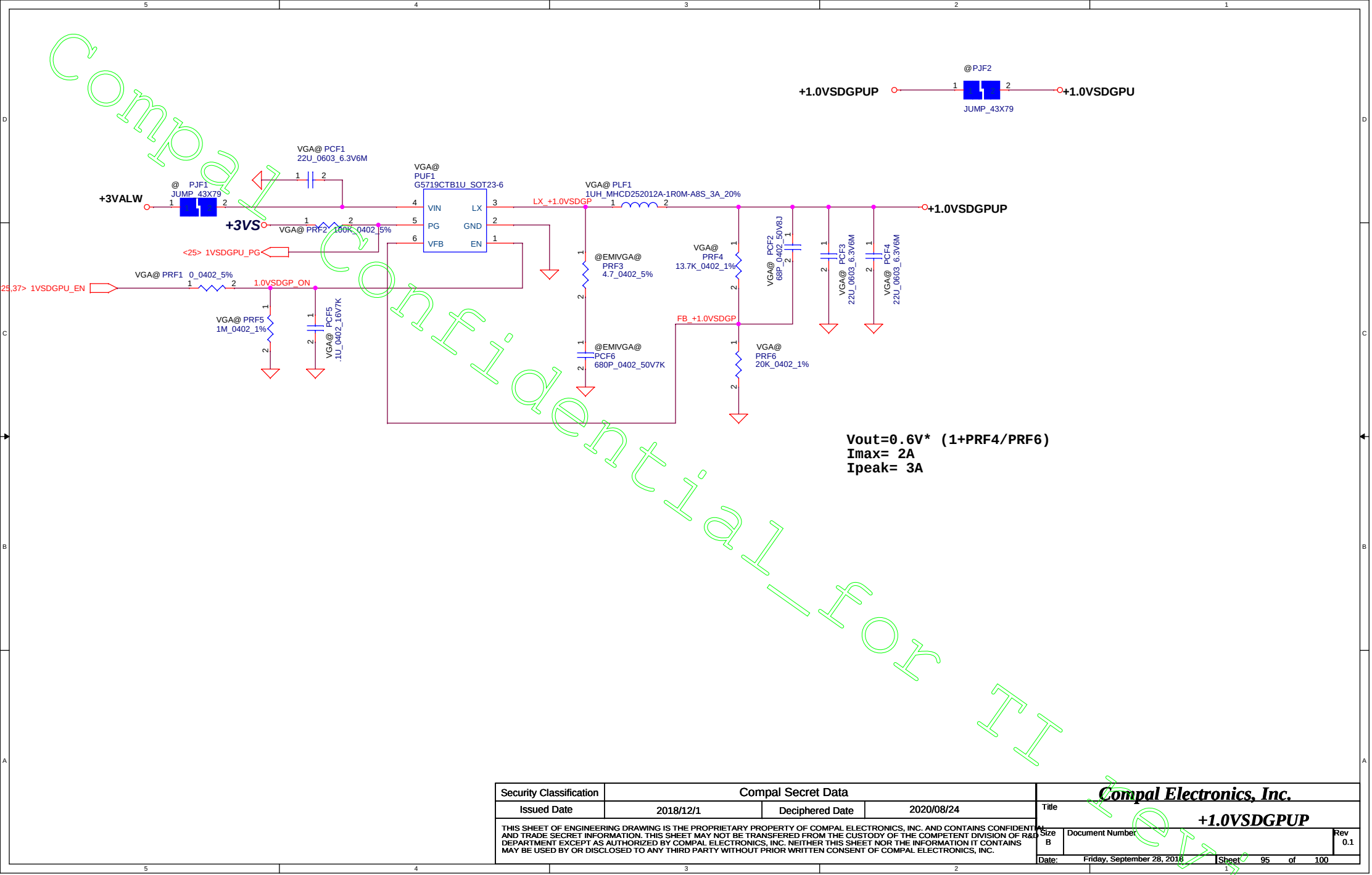

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Compal Electronics, Inc.

Title: **+1.0VSDGPUP**

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 95 of 100

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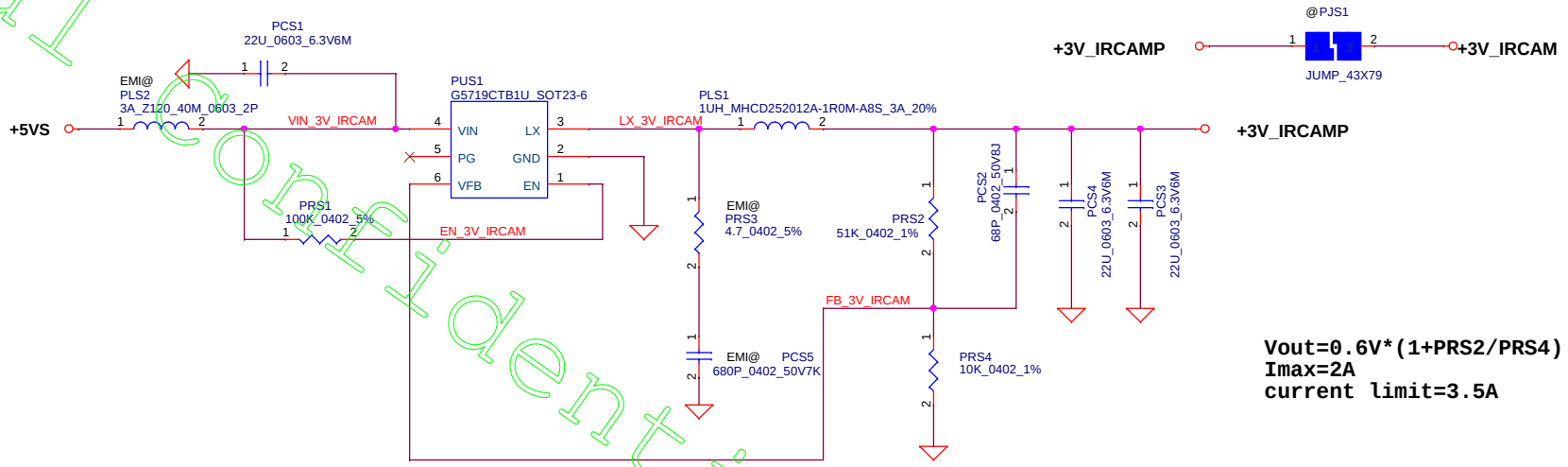

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Compal Electronics, Inc.

Title: +3V_IRCAMP

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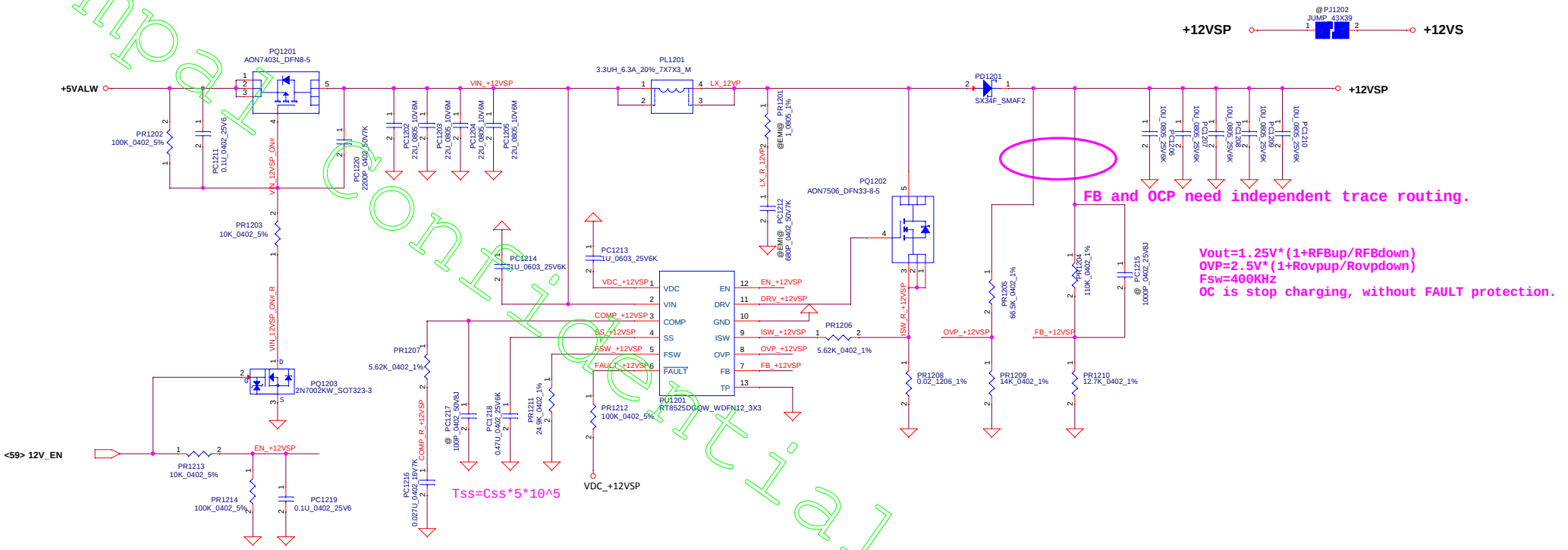
Date: Friday, September 28, 2018 | Sheet 96 of 100



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Title: **+12VS**

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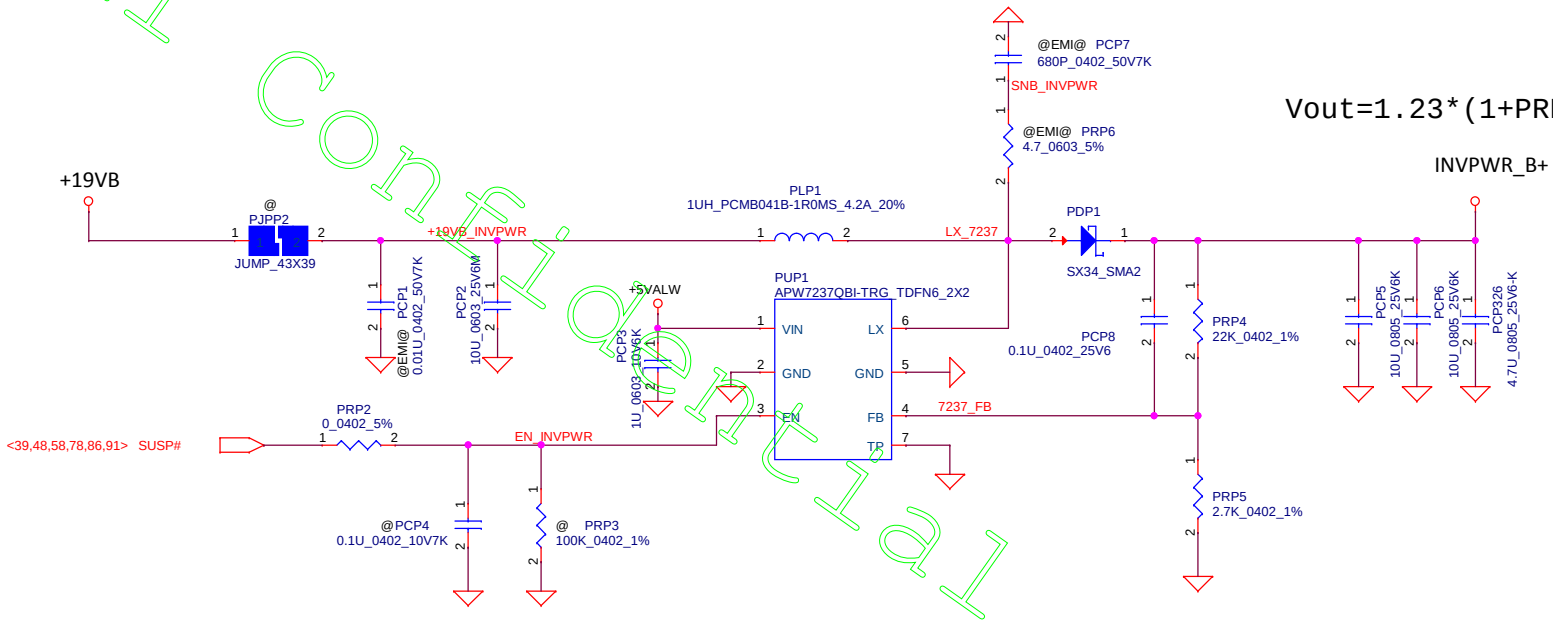

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Title: **INVPWR_B++**

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Title: **PIR**

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Title: **Reserve for PWR**

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